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9508 MICROSYSTEM EMULATOR

USERS MANUAL ADDENDUM

8048/49/21/41A OPTION

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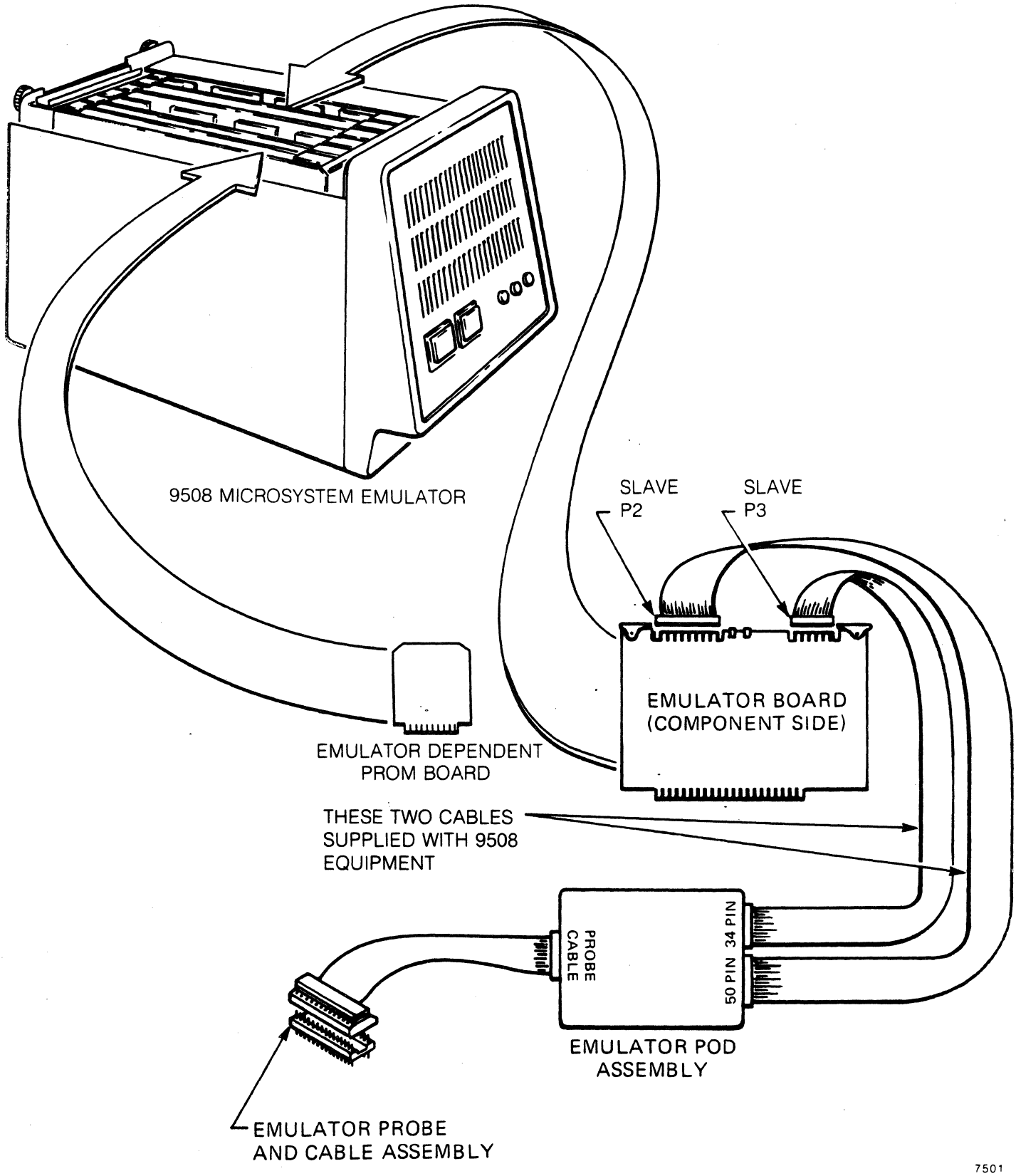

8048/49/21/41A Emulator Option Components

WARNING:

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The following procedures may help to alleviate the Radio or Television Interference Problems:

1. Reorient the antenna of the receiver receiving the interference.

2. Relocate the equipment causing the interference with respect to the receiver (move or change relative position).

3. Reconnect the equipment causing the interference into a different outlet so the receiver and the equipment are connected to different branch circuits.

4. Remove the equipment from the power source.

NOTE:

The user may find the following booklet prepared by the FCC helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Printing Office, Washington, D.C. 20402. Stock No. 004-000-00345-4.

This addendum to the 9508 MicroSystem Emulator Users Manual describes the capabilities, functions and operations of the 8048/49/21/41A Emulator Option. This option contains the necessary hardware components to configure the 9508 MicroSystem Emulator for testing/debugging user programs and hardware that are developed to support the 8048/49/21/41A Microprocessor chip. This addendum includes procedures for installing the optional equipment at the user's site and operating the 9508 MicroSystem Emulator to exercise the 8048/49/21/41A hardware/software functions. This addendum is to be used with, and inserted in back of the 9508 MicroSystem Emulator Manual.

The material in this addendum is up-to-date at the time of publication, but is subject to change without notice.

Copies of this publication and other Millennium publications may be obtained from the Millennium sales office or distributor serving your locality.

RELATED PUBLICATIONS

Manuals:

- 9508 MicroSystem Emulator Users Manual

Application Notes:

- Diagnostic Programming for Microprocessor Based Systems
- Guide to Testing Microprocessor Unit Data Sheet

Data Sheets:

- Intel 8048, 8049, 8021 and 8041A Microprocessor Unit Data Sheets

If you require any assistance on this product, please call Millennium Systems Customer Service on the toll-free, hot-line numbers listed below:

National	(800) 538-9320/9321
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8048/49/21/41A EMULATOR OVERVIEW

This manual explains the operation of the 8048/49/21/41A Emulator Option for the 9508 MicroSystem Emulator.

The 8048/49/21/41A Emulator Option permits the user of 9508 equipment to expand the emulation capability to support microprocessor-based systems that are configured with devices of the 8048, 8049, 8021 and 8041A microprocessor chip groups. These groups consist of the following devices:

Group Name	Devices	Memory
8048	8048	1KX8 ROM, 64X8 RAM
	8048	With Expanded Memory
	8748-4, 8748-8	1KX8 EPROM, 64X8 RAM
	8035, 8035-4, 8035-8	64X8 RAM
8049	8049, 8049-6	2KX8 ROM, 128X8 RAM
	8049, 8049-6	With Expanded Memory
	8039, 8039-6	128X8 RAM
8021	8021	1KX8 ROM, 64X8 RAM
8041A	8041A	1KX8 ROM, 64X8 RAM
	8741A	1KX8 EPROM, 64X8 RAM

These on-chip RAM and ROM resources, however, are not used by the 9508 for emulation because these memory functions are reconstructed externally by RAM circuits located in the emulator interface hardware.

Emulation on the 9508 system is accomplished in real-time processing and allows the user to perform the following functions:

- Set Breakpoints for hardware and software
- Step through user programs
- Run display or modify user programs in the unit under test (UUT)
- Display and alter contents in registers, memory, and I/O ports
- Perform real-time trace and record the events
- Specify memory mapping and clock modes
- Display emulation environment
- Use emulator memory to make patches for program ROM

INTRODUCTION

The 9508 MicroSystem Emulator with the 8048 Family Emulator Option installed, contains two microprocessors as follows:

1. The MC6800 control microprocessor is located on the control processor board that drives the 9508 system; it supervises system resources and executes commands that control the system processing functions for emulation.

2. The 8035 or 8039 microprocessor used in the target system is located, respectively, on the 8041A or 8048 pod interface circuit board inside the Emulator Pod Assembly; it executes the users software and activates user hardware functions. The emulator pod contains special circuits that adapt the emulator microprocessor to operate identically to the UUT system microprocessor.

HARDWARE DEBUGGING

The Emulator Pod Assembly interfaces with the users unit under test via the Probe and Cable Assembly (see figure 1-1). This cable is terminated by a 40-pin probe for the 8048/49/41A groups, or a 28-pin probe for the 8021 group. The probe plugs into the microprocessor socket of the unit under test (UUT). By replacing the users microprocessor in the UUT with the emulator probe, the user can execute UUT programs under the control of the 9508 assembly language programs that reside in the following memory areas:

9508 Emulator RAM
UUT ROM

This feature allows rapid debugging of both UUT hardware and software. Figure 1-1 shows the 9508 MicroSystem Emulator connected to a UUT.

SOFTWARE DEBUGGING

Any 8048/49/21/41A executable object program can be executed/tested using the 9508 MicroSystem Emulator. Such a program may have been written in 8048/49/21/41A Assembly Language and appropriately assembled and linked at a host software development system and then downloaded from the host to reside in the 9508 emulator memory. The software system can be tested and debugged by the emulator without interfacing to a user hardware system.

1. The user can make patches to the program using assembly language mnemonics for opcodes. The emulator In-Line Assembler will automatically translate these mnemonics to the machine language used by the target system. Memory must be mapped to the 9508 RAM.

2. Likewise, the emulator In-Line Disassembler allows the user to display memory using the assembly language mnemonics.

3. The users software can be debugged using the 9508 memory and emulator, or the software can be tested using only the memory in the UUT.

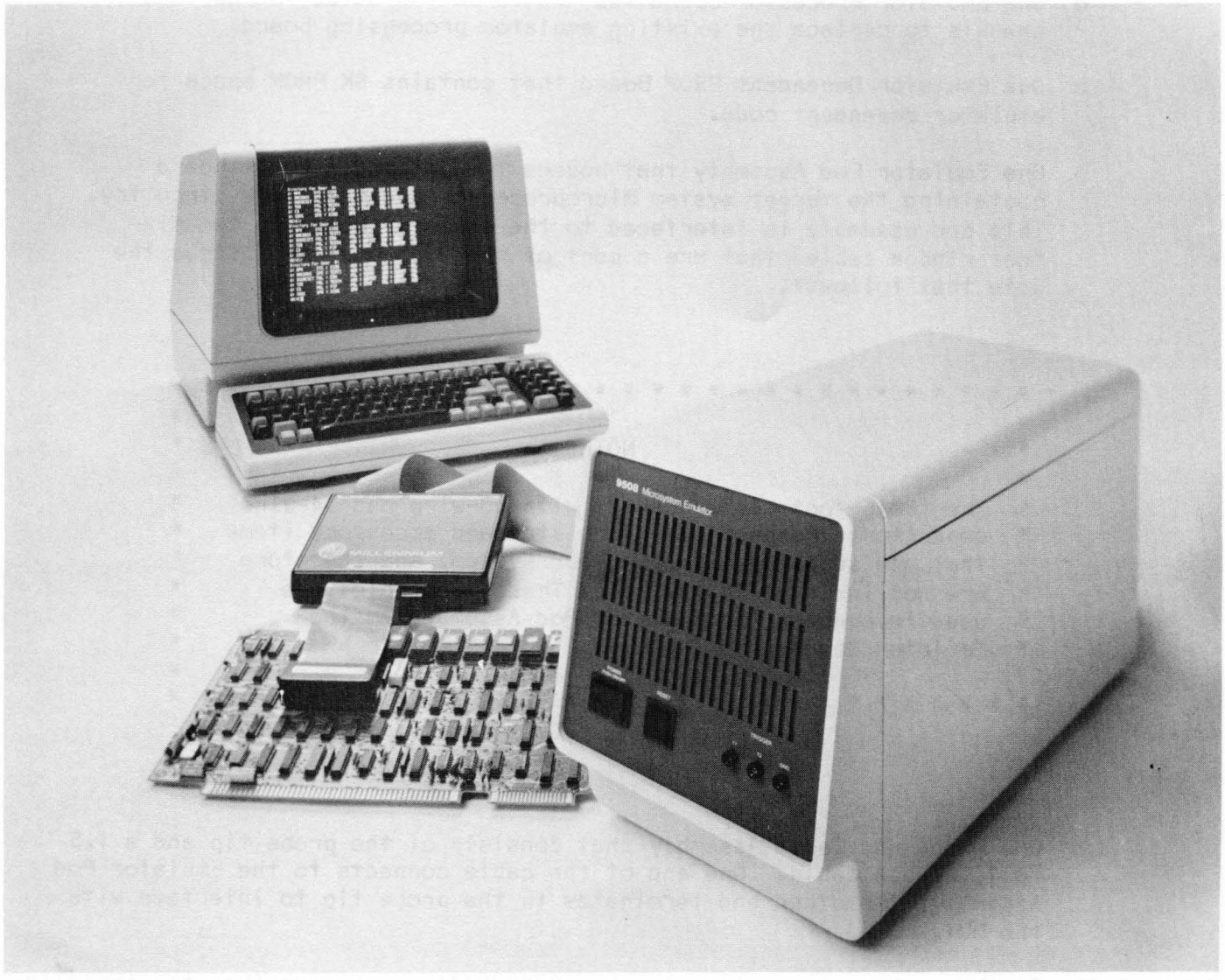


Figure 1-1. 9508 MicroSystem Emulator Connected to a Unit Under Test

DESCRIPTION OF 8048/49/21/41A EMULATOR OPTION COMPONENTS

The 8048/49/21/41A Emulator Option contains the following items which are packaged in a kit for installation by the user in his 9508 system hardware.

- One Emulator Processor Board that is to be installed in the 9508 chassis to replace the existing emulator processing board.
- One Emulator Dependent PROM Board that contains 8K PROM space for emulator dependent code.
- One Emulator Pod Assembly that houses the printed circuit board containing the target system microprocessor and interface circuitry. This pod assembly is interfaced to the emulator board by two six-foot ribbon cables that are a part of the 9508 equipment (*see the note that follows).

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                               *
*                            NOTE                               *
*                                                               *
*  The two 6-foot ribbon cables with 50-wire and 34-wire        *
*  conductors, respectively, are standard accessory items       *
*  that are supplied with the 9508 system, and therefore        *
*  are not included in the kit.  These two cables are           *
*  used to connect the Emulator Pod Assembly to the             *
*  Emulator Board.                                              *
*                                                               *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

- One Probe and Cable Assembly that consists of the probe tip and a 1.5 foot, ribbon cable. One end of the cable connects to the Emulator Pod Assembly; the other end terminates in the probe tip to interface with the UUT.
- One Users Manual (Publication No. 87000077) which describes the installation and operation procedure for the 8048/49/21/41A Emulator Option.

Due to design and operational requirements, the 8048 Emulator Option actually requires three distinct configurations. These configurations are grouped as follows:

- 8048 (comprising the 8035, 8039, 8048, 8748, and 8049)
- 8021
- 8041A (comprising the 8041A and 8741A)

Each configuration comprises separate and distinct components, some of which may be intermixed. These components are given in table 1-1.

Table 1-1. Emulator Components

Device Group	Main Emulator Board P/N	8048 Pod P/N	8048 Probe P/N	8041A Pod P/N	8021 Probe P/N
8048/49	13000125	15000148	15000147	--	--
8021	13000125	15000148	--	--	15000179
8041A	13000125	--	15000147	15000178	--

Depending upon which version of the 8048 Emulator Option is ordered, expansion to any of the other versions is simplified since some of the components are common. As an example, if the emulator is initially ordered for the 8048 and later the need for 8021 emulation arises, only the 8021 probe (part number 15000179) need be ordered.

Information on how to order the 8048/49/21/41A Emulator Option as a complete package or individual parts of the package is presented in Appendix E.

DIFFERENCES IN EMULATOR AND ON CHIP FUNCTIONS

Except for the electrical and timing differences indicated in the specifications of Appendix A, there are only a few cases where the 8048/49/21/41A emulator is functionally different from the 8049/49/21/41A microprocessor in the Unit Under Test. These differences are summarized in the following list, with expanded coverage provided in Chapter 3:

1. The 8048, 8049 and 8021 are emulated using an 8039 microprocessor. In normal operation, the 8021 Program Counter rolls over to 0H after reaching 3FFH. Because the device is being emulated using an 8039, the Program Counter rollover does not occur until 7FFH.

   Similarly, the emulation of Internal Data Memory is affected. A register pointer for an 8048 or 8021 normally rolls over at 3FH, but when emulated by an 8039 it rolls over at 7FH. For this reason, the user must take care not to access Internal Data Memory locations 40H through 7FH when emulating the 8048 or 8021. This may be checked by using the XDATA command to set the memory within this range to some known value, executing the program, and then use the DDATA command to examine the memory to see if it has been changed.

2. The 9508 system allows the user to replace or map portions of the UUT address space using RAM contained in the system. Because the 8048 and 8049 have two address spaces, Program Memory and External Data Memory (both based at 0H), the difficulty of using one address space to emulate a processor having two address spaces is resolved by establishing the following conventions:

   a. Addresses in the range 0H-FFFH cause Program Memory to be accessed.

   b. Addresses in the range 1000H-10FFH cause External Data Memory to be accessed. Whenever External Data Memory is accessed, the emulator adds 1000H to the address.

   The MAP command and Real-Time Trace Buffer are affected by these conventions. Because of its architecture, the 8048 Family of devices have no instructions that write to Program Memory. As a result, portions of Program Memory not mapped to the 9508 System cannot be modified. 9508 commands which attempt to modify memory mapped to the UUT fail. These commands include:

   ASM
   EXAM
   FILL
   MOVE
   RHEX

   Table 1-2 lists the commands and their restrictions.

Table 1-2. Commands and Restrictions

COMMAND	PROGRAM MEMORY		EXTERNAL DATA MEMORY	INTERNAL DATA MEMORY
	MAPPED TO UUT	MAPPED TO 9508		
ASM		X		
BIAS	X	X	X	
BREAK	X	X	X	
DDATA			X	X
DISM	X	X		
DUMP	X	X	X	
EVENT	X	X	X	
EXAM	X (READ)	X (R/W)	X	
FILL		X	X	
GO	X	X		
MAP	X	X	X	
MOVE	X (READ)	X (R/W)	X	
RHEX		X	X	
TRACE	X	X		
WHEX	X	X	X	
XDATA			X	X

NOTE: X represents a valid command.

3. Real Time Emulation of the Timer/Counter is not supported whenever the emulator is not executing in real-time.

4. For the 8041A, there are a number of flags which are displayed to the user in Flag Byte 2 of the TRACE line. These include:

   Input Buffer Full (IBF)
   Output Buffer Full (OBF)
   Status ST7-ST4
   EN FLAGS
   EN DMA

   The information displayed is correct only in User Mode and not System Mode.

   The F1, IBF, and OBF flags may be changed asynchronously by a controlling processor. The values displayed are the values read immediately after the last user instruction was executed.

5. When emulating an 8041A, only a RET instruction can be used to return control to the calling program from a subroutine. The RETR instruction can only be used to return control from an interrupt service routine.

6. A false break indication occurs if an interrupt and an instruction fetch on a breakpoint location (set using the BREAK or GO commands) occur simultaneously. Once the breakpoint has been serviced, the program execution resumes with the interrupt service routine. After the interrupt routine restores and returns, the actual breakpoint occurs.

INSTALLATION

GENERAL

This chapter describes the installation of the 8048/49/21/41A Emulator Option components in the 9508 MicroSystem Emulator unit. The installation involves replacing the existing components in the card cage with the 8048/49/21/41A Emulator Board and the 8048/49/21/41A Emulator Dependent PROM Board supplied in the Emulator Option Kit. The existing emulator pod assembly and probe cable assembly are also replaced with corresponding components from the 8048/49/21/41A Emulator Option Kit.

Only one emulator board and dependent PROM Board may be installed in the card cage at a time. For example, if a Z80 type emulator board and its corresponding dependent PROM board are presently installed in the 9508 chassis, then both boards must be removed and the 8048/49/21/41A boards installed in their place.

Approximately ten different types of microprocessor emulators are available for the 9508. Each type of emulator board interfaces with its corresponding emulator dependent PROM board and pod assembly. These parts contain unique hardware, logic and software routines that support a specific type of microprocessor and cannot be interchanged with similar components used for other types of emulators. For example, the Z80 or 6800 emulator components will not function with the 8048/49/21/41A emulator, or vice versa, and a mismatch could cause damage to the components. It is therefore necessary to ensure that all installed emulator components correspond to the type of microprocessor associated with the target system.

UNPACKING AND INSPECTION

All of the hardware items that are necessary for a user to install and operate the 8048/49/21/41A Emulator Option is contained in a packaged kit. Two printed circuit boards are provided to be installed in the 9508 chassis. The emulator pod assembly and probe cable are to be connected in the system as described in the procedure which follows.

Table E-1 in appendix E contains a list of individual parts and assemblies that are supplied in the kit. Use this table and the shipping papers to verify that all items are received.

If the equipment received from the carrier is incomplete or damaged, do not install the equipment. File a claim with the shipping firm immediately, and notify Millennium System's Customer Service department at once. Millennium will arrange for repair or replacement of the equipment without waiting for settlement of the claim against the carrier.

If the equipment must be returned to Millennium, attach a tag showing the owner, address, serial number, and a description of the failure. The original shipping carton and packing material should be reused with the RMA (Returned Material Authorization) number prominently displayed. An RMA number can be obtained by calling Customer Service on the toll-free, hot-line numbers listed in the Preface.

INSTALLATION

Millennium System's Technical Support Representatives and Customer Engineers are available to provide consultation and assistance on request.

MAINTENANCE AND SERVICE POLICIES

Unless notified to the contrary, any claims for operations assistance and/or service will be provided by Millennium Systems, Inc., from its plant in Cupertino, California. Should assistance be required, call Customer Service.

SPECIAL ON-BOARD CONNECTIONS

The interface board inside the pod contains DIP switches that are set by the manufacturer to support a specific member of the 8048 family. These DIP switch settings are described in the back of this chapter.

INSTALLATION PROCEDURE

Before any kind of system testing is performed, the 8048/49/21/41A emulator board and emulator dependent PROM board must be installed in the 9508 chassis. Refer to figures 2-1 and 2-2, and perform the following step-by-step procedures:

1. Remove power from the 9508 system and the UUT by pressing the POWER ON/OFF switch.

2. Loosen the two retaining screws at the rear of the chassis and remove the top access cover.

3. Locate the emulator board in the card cage. It can be identified by the name of the microprocessor that is labeled at the top of the board (Z80, 8080, 8085, etc.). It is located in the fifth slot from the left side of the card cage as shown in figure 2-1.

4. Disconnect the two ribbon cable edge connectors (SLAVE P2 and SLAVE P3) from the emulator board.

5. Using both hands, grasp the release tabs on each side of the emulator board and simultaneously pull out on the tabs so that the board is pulled out of its connector.

6. Remove the emulator board from the 9508 and store.

7. Insert the 8048/49/21/41A emulator board into the same slot of the card cage and simultaneously push down with both hands until it is fully seated.

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                       *
*                       CAUTION                         *
*                                                       *
*   Be careful not to damage the ribbon cable           *
*   connectors when installing the emulator board.      *
*                                                       *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

8. Connect the two ribbon cable connectors (Slave P2 and Slave P3) onto the P2 and P3 mating edge connectors on the emulator board. Carefully fold and route the ribbon cables through the horizontal slot at the rear of the chassis. The cables must be positioned flat against the slot to avoid interference when the top access cover is installed.

9. Disconnect the four-wire cable from the existing emulator dependent PROM board located at the upper left-hand front corner of the chassis. Remove the existing PROM board and insert the emulator dependent PROM board from the kit in its place with the component side facing the interior of the chassis. Connect the four-wire cable to the 4-pin connector at the top of the PROM board.

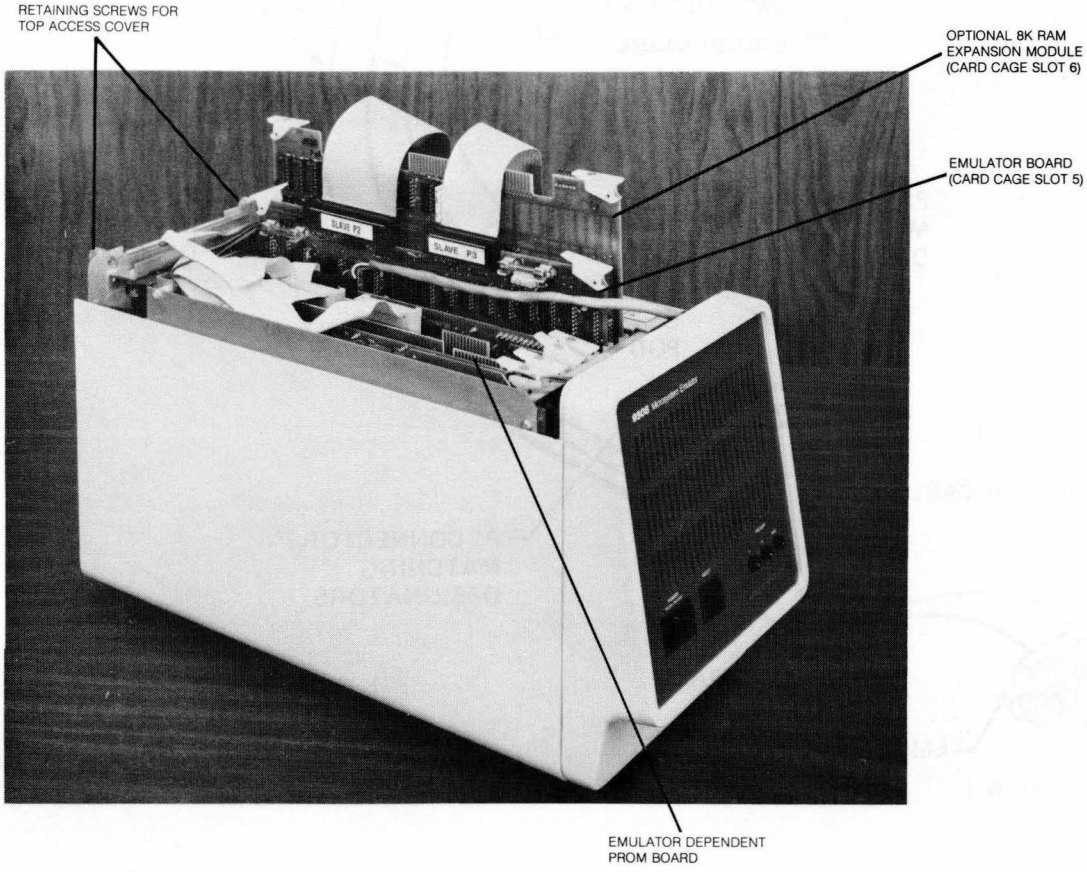

RETAINING SCREWS FOR TOP ACCESS COVER
OPTIONAL 8K RAM EXPANSION MODULE (CARD CAGE SLOT 6)
EMULATOR BOARD (CARD CAGE SLOT 5)
SLAVE P2
SLAVE P3
EMULATOR DEPENDENT PROM BOARD

Figure 2-1. Location of Emulator Board and Emulator Dependent PROM Board in 9508 Chassis

```
* * * * * * * * * * * * * * * * * * * * * * *
*                                             *
*                  WARNING                    *
*                                             *
*   Installing the cables incorrectly may     *
*   result in damage to the emulator board    *
*   or the pod.                               *
*                                             *
* * * * * * * * * * * * * * * * * * * * * * *
```

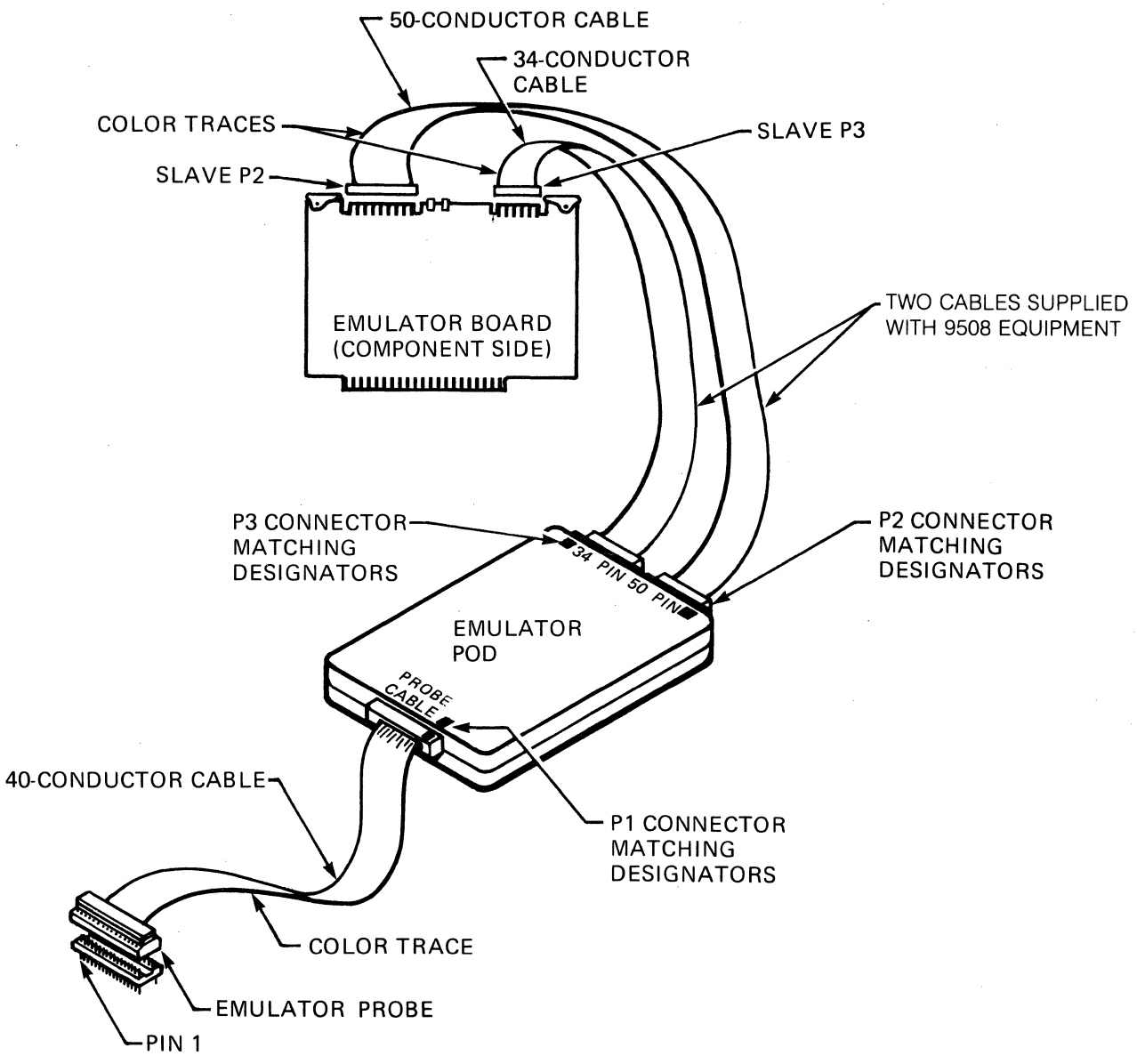


Figure 2-2. Connecting the 8048/49/21/41A Emulator Pod

10. Install the top access cover and tighten the two retaining screws at rear of the chassis.

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                       *
*                       CAUTION                         *
*                                                       *
*  The top access cover must be replaced to             *
*  provide proper air circulation before AC             *
*  power is applied.  Ensure that the top               *
*  access cover is properly secured.  The               *
*  buildup of heat due to improper air flow             *
*  will result if the top cover is not                  *
*  secured.                                             *
*                                                       *
* * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

11. Disconnect the existing emulator pod from the emulator cables and connect the 8048/49/21/41A emulator pod. Match the P2 and P3 socket designators on the pod with the corresponding designators on the cables and connect the cables.

12. Connect the emulator probe cable with attached probe to edge connector P1 on the emulator pod.

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                       *
*                       CAUTION                         *
*                                                       *
*  If the  pod is plugged in incorrectly, it could      *
*  damage the pod or the emulator board.                *
*                                                       *
* * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

13. Remove the 8048 Family microprocessor from the UUT socket and plug the emulator probe tip into the microprocessor socket. Make sure that pin 1 of the socket is aligned with pin 1 of the probe tip.

14. After checking all connections, turn on power to the 9508 and UUT.

OPTIONAL USER DIP SWITCH SETTINGS

The 8041A pod interface board is of a fixed configuration and contains no switches or jumpers; however, the 8048 pod interface board contains DIP switches that can be modified by the user. These on-board DIP switches shown in figure 2-3 are adjusted by the manufacturer for emulation of a specific member of the 8048 family. These factory settings, however, may be changed by the user to adapt the emulator for emulation of another member of the 8048 Family. If the emulator option is already installed, the power must be removed from the 9508 equipment before changing the DIP switch settings.

The DIP switch is located on the printed circuited board within the 8048 Emulator Pod. The only tool required to gain access to the emulator board is a small bladed screwdriver.

1. Remove all exterior cable connections from the 8048 Emulator Pod.
2. Use the screwdriver to remove the four (4) screws holding the emulator pod together.
3. Remove the pod back cover and carefully remove the printed circuit board.
4. Refer to Table 2-1 to select the emulator switch configuration that matches the device to be tested.
5. After the DIP switch has been change to the proper configuration, replace the printed circuit board in the emulator case, replace the back cover, insert and secure the four screws.

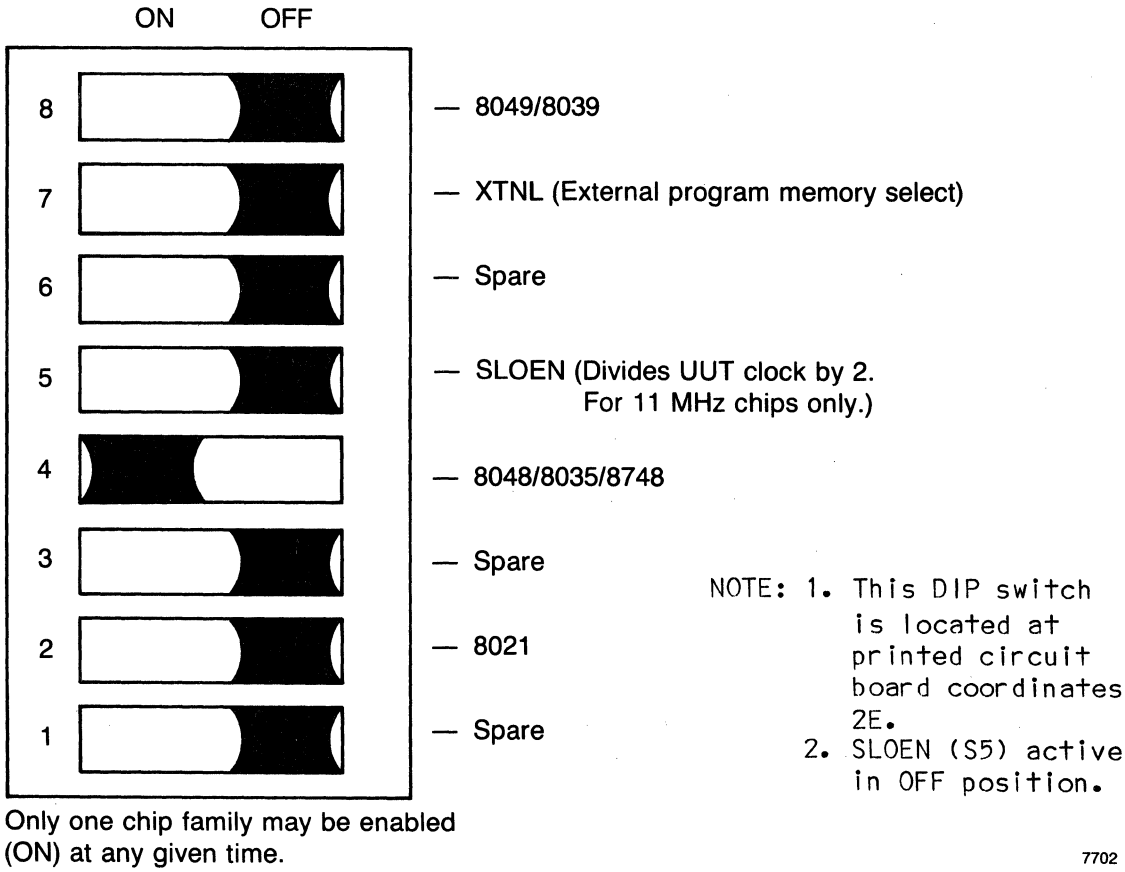


Figure 2-3. On-Board DIP Switches

Table 2-1. DIP Switch Settings
(See Note 4)

DEVICE	DIP SWITCH NUMBER							
	1	2	3[1]	4	5[2]	6[1]	7[3]	8
8049 (11 MHz)	0	0	0	0	0	0	0	1
8049 W/External Program Memory	0	0	0	0	0	0	1	1
8039 (11MHz)	0	0	0	0	0	0	1	1
8039-6 (6 MHz)	0	0	0	0	1	0	1	1
8048/8748	0	0	0	1	1	0	0	0
8048 W/External Program Memory	0	0	0	1	1	0	1	0
8035	0	0	0	1	1	0	1	0
8021	0	1	0	0	1	0	0	0

Notes:

1 - Switches 1, 3 and 6 are spares and should remain in the OFF position.

2 - Switch 5 is the SLOEN switch, and its active position is OFF. It is set whenever the clock rate is greater than 6 MHz. SLOEN divides the clock rate by two whenever memory external to the UUT is accessed. If no memory is mapped, the user notices no difference; however, the switch must still be set because during the register save and restore routines system or utility memory will be accessed.

3 - Switch 7 is the External Program Memory enable switch, and its active position is ON. When the switch is active, the display indicates a processor type of 8048 (or 8049) with Expanded Memory for the respective devices. When the 8035 is the processor being emulated, the display indicates a processor type of 8048 with Expanded Memory, and when the 8039 is the processor being emulated, the display indicates a processor type of 8049 with Expanded Memory.

4 - The DIP switches are contained only on the 8048/49/21 Emulator Pod board; therefore, table 2-1 is applicable only to the 8048/49/21 Emulator Pod Board.

FUNCTIONAL DESCRIPTION

GENERAL

This chapter presents a functional description of the 8048/49/21/41A Emulator Option.

The emulator supports microprocessor-based systems that employ the 8048, 8748, 8035, 8049, 8039, 8021, 8041A and 8741A chips. These devices comprise the 8048 Family, which are examples of the Harvard architecture in which there are several address spaces, one for instructions and read-only data and another for temporary (read/write) data. The 8048 family has an I/O space arranged as follows:

Port 0 -- 8 Bits
Port 1 -- 8 Bits
Port 2 -- 8 Bits

Port 4 -- 4 Bits
Port 5 -- 4 Bits
Port 6 -- 4 Bits
Port 7 -- 4 Bits

It should be noted that if there is any offboard Program Memory, the user should not use the low nibble of Port 2 for input or output data.

```
OUTL P2,A
```

is not completely emulated when there is offboard Program Memory.

If data is latched in the quasi-bidirectional static port and external program memory is accessed, the port data must be unlatched so the address can be passed to the UUT before the trailing edge of ALE. Since it is indeterminate as to when ALE will go low, the port should not be unlatched until ALE does go low - at which time it is too late for the UUT to latch the address.

Because of the Catch-22 nature of the situation, the absolute emulation of Port 2 is affected only when using expanded program memory. For this condition, Port 2 will always be unlatched. It therefore falls upon the UUT to externally latch the Port 2 data on the rising edge of ALE in order retain that data.

OPERATING CONCEPT

Circuits in the interface pod assembly reconstruct the internal 8048/49/21/41A so that the emulator can be used to select, examine and operate the CPU functions in a real-time test environment. Primary functions of the CPU are:

1. To fetch instructions from memory in a sequential manner until instructed otherwise.

2. To perform the operation called out by the instruction.

3. To control the interpretation and execution of the instruction.

4. To monitor and control the remaining elements of the system.

5. To control the flow of data throughout the system.

The emulator allows the user to manipulate CPU functions for the following purposes:

- o examining registers
- o changing the register contents
- o transferring data
- o controlling the execution of the user's program
- o recording the status of the resulting operations
- o examining memory
- o changing memory contents
- o reading I/O ports
- o writing I/O ports

8048/49/21/41A INSTRUCTIONS

The 8048/49/21/41A instruction set is described in appendix C. These instructions may be classified into the following major groups:

- o Data Transfers
- o Accumulator Operations
- o Register Operations
- o Flags
- o Branch Instructions
- o Subroutines
- o Timer Instructions
- o Control Instructions
- o Input/Output Instructions

OPERATING SPEED

The 8048 Emulator Pod microprocessor is capable of operating at a maximum speed of 11 MHz in the user memory space. When operating at speeds in excess of 6 MHz, the SLOEN DIP-switch must be switched to its active position. This allows access to UUT memory at the UUT clock frequency, and access to the System memory at the UUT clock frequency divided by two.

FORCED JUMP LOGIC

When a jump command is issued by the System Processor module, the Forced Jump logic steps the Emulator Processor module through a sequence of operations.

The Forced Jump logic consists of a six byte sequence and a control and instruction ROM. The instruction sequence of the jump cycle depends upon whether the microprocessor is being Force Jumped to a program or has been breakpointed. The sequence for a jump to program execution is as follows:

1. JMP TO OBJECT PAGE LOC 0
2. RESTORE THE BANK SELECT STATUS
3. RESTORE THE INTERNAL COUNTER MODE
4. BRANCH TO OBJECT LOCATION

The restoring of bank select and the counter mode is achieved via the Aux command byte and the sequencing ROM.

The sequence for a breakpoint or single cycle interrupt is as follows:

1. STOP THE INTERNAL COUNTER
2. JMP TO PC NXT
3. JMP TO PC NXT
4. NOP (OUTPUT PC NXT)

Note that the primary purpose of the sequencer when breakpointed is to successfully output PC next. The additional cycles of this sequence are to allow a timer interrupt to occur before PC next is output if the timer interrupt is enabled.

EMULATOR DEPENDENT COMMANDS

The 8048/49/21/41A emulator dependent commands initiate and control the emulation processing the unique characteristics of the 8048 Family microprocessor used in the target system. These characteristics are established by the CPU architecture and chip design features which include the following:

- o CPU Instruction Set Mnemonics and Opcodes
- o CPU Register Identification and Functions
- o I/O Port Configurations and Control
- o CPU External System Controls

Command Description

The 9508 MicroSystem Emulator employs 28 basic commands for system operations. The following basic commands are configured by the software to control emulation processing for the 8048/49/21/41A chip functions:

COMMAND NAME	MINIMUM ENTRY
ASM	A)sm
DDATA	DD)ata
DISM	DI)sm
DRT	DR)t
PORT	P)ort
RESET	RES)et
REG	REG
REGBRK	REGB)rk
STATUS	S)tatus
XDATA	XD)ata

The use of these commands for 8048/49/21/41A emulation processing is described in subsequent paragraphs. In the interest of continuity of the example program, the DUMP command is included in the illustrations.

ASM Command

The A)sm command is used to modify instructions and data in program memory. The 8048/49/21/41A Instruction Set mnemonics and syntax described in appendix C can be specified in the input instead of the hexadecimal opcode. The operand value for addresses and data can only be set in hexadecimal values.

In the following example, the A)sm command is used to prepare a translation table in Page 3 of Program Memory. This table translates ASCII to binary for 0-9 and A-F.

```
D>A)sm 330
     0330 BYTE 0,1,2,3,4,5,6,7,8,9
     033A BLOCK 7
     0341 BYTE 0A,0B,0C,0D,0E,0F
     0347
```

The A)sm command is then used to prepare the program instructions as follows:

```
D>A)sm 20
     0020 MOV R2,#10
     0022 MOV R0,#30
     0024 MOV A,@R0
     0025 MOVP3 A,@A
     0026 MOVX @R0,A
     0027 INC R0
     0028 DJNZ R2,24
     002A JMP 2A
     002C
```

XDATA Command

The XD)ata command provides user address to internal and external data memory, and is similar in operation to the EX)amine command. The syntax of the XD)ata command is as follows:

XD)ata {I / X} [addr]

The first parameter, a required parameter, selects either internal data (I) or external data (X). The second parameter selects the address at which the examine and change operation is to begin. The second parameter default is 0.

In the following illustration, the XD)ata command is used to put ASCII data into Internal Memory.

```
D>XD)ata I 30
     INT  30=00-30  01-31  02-32  03-33  77-34  9D-35  79-36  0A-37
     INT  38=10-38  00-39  40-41  00-42  DB-43  BF-44  C2-45  4D=46
     INT  40=25-
```

DISM Command

The DI)sm command translates hexadecimal program memory data to an assembled mnemonic line form. The 8048/49/21/41A Instruction Set mnemonics are used in the display format. Areas of memory that are unrecognizable in the form of instruction mnemonics are displayed as question marks (e.g. ???=). The following example indicates the output display for data that was assembled by the A)sm command:

```
D>DI)sm 20 2A
     ADDR   OBJECT          INSTRUCTION
      0020  BA 10           MOV    R2,#10
      0022  B8 30           MOV    R0,#30
      0024  F0             MOV    A,@R0
      0025  E3             MOVP3  A,@A
      0026  90             MOVX   @R0,A
      0027  18             INC    R0
      0028  EA 24          DJNZ   R2,0024
      002A  04 2A          JMP    002A
```

The following example indicates the result of executing the program. The ESC key can be used to stop emulation.

```
D>GO 20 UNTIL 2A TRACE ALL
  LOC  MNEM   OPRD/EADDR A C AC F01 TF TCR SP RB R0 R1 R2 R3 R4 R5 R6 R7 PCNEXT
  0020 MOV    R2,#10     CC 0  0  00  0  00 08 0 00 00 10 00 00 00 00 00   0022
                                                1 00 00 00 00 00 00 00 00
  0022 MOV    R0,#30     CC 0  0  00  0  00 08 0 30 00 10 00 00 00 00 00   0024
                                                1 00 00 00 00 00 00 00 00
  0024 MOV    A,@R0      30 0  0  00  0  00 08 0 30 00 10 00 00 00 00 00   0025
               00                               1 00 00 00 00 00 00 00 00
  0025 MOVP3  A,@A       00 0  0  00  0  00 08 0 30 00 10 00 00 00 00 00   0026
                                                1 00 00 00 00 00 00 00 00
  0026 MOVX   @R0,A      00 0  0  00  0  00 08 0 30 00 10 00 00 00 00 00   0027
               00                               1 00 00 00 00 00 00 00 00
  0027 INC    R0         00 0  0  00  0  00 08 0 31 00 10 00 00 00 00 00   0028
                                                1 00 00 00 00 00 00 00 00
  0028 DJNZ   R2,0024    00 0  0  00  0  00 08 0 31 00 0F 00 00 00 00 00   0024
                                                1 00 00 00 00 00 00 00 00
  0024 MOV    A,@R0      31 0  0  00  0  00 08 0 31 00 0F 00 00 00 00 00   0025
               00                               1 00 00 00 00 00 00 00 00
  0025 MOVP3  A,@A       01 0  0  00  0  00 08 0 31 00 0F 00 00 00 00 00   0026
                                                1 00 00 00 00 00 00 00 00
  0026 MOVX   @R0,A      01 0  0  00  0  00 08 0 31 00 0F 00 00 00 00 00   0027
               00                               1 00 00 00 00 00 00 00 00
    .
    .
```

Note: For the DI)sm and DR)t commands, it is impossible to know the value of the Memory Bank Flag (MBF for 8048 and 8049) when an instruction is executed. Therefore, when disassembling from memory or the real time trace buffer, we assume a value of 0 for the Memory Bank Flag. All addresses for JMP or CALL instructions will fall in the range 0-7FFH.

DUMP Command

The D)ump command displays program memory contents in hexadecimal and ASCII format. The display of data that was assembled using the A)sm command is presented in the following example:

```
D>D)ump  330  340
     ADDR  0  1  2  3  4  5  6  7   8  9  A  B  C  D  E  F   ASCII
     0330=00 01 02 03 04 05 06 07   08 09 01 07 08 0E 03 4F   ........ .......0
     0340=60 0A 0B 0C 0D 0E 0F 21   00 2C 05 40 02 44 04 08   '......! .,.@.D..
```

DDATA Command

The DD)ata command is similar in operation to the D)ump command, and provides displays of internal or external data memory. It's syntax is as follows:

DD)ata { I / X } [low addr [high addr]]

The first parameter, a required parameter, selects either Internal (I) or External (X) Data memory. The second parameter selects the starting address. If not specified, both it and the third parameter default to their previous values. The third parameter selects the ending address. Its default value is the second parameter.

In the following example, the DD)ata command is used to display the data previously placed in Internal Memory by use of the XD)ata command.

```
D>DD)ata I  30
   ADDR  0  1  2  3  4  5  6  7    8  9  A  B  C  D  E  F   ASCII
 INT 30=30 31 32 33 34 35 36 37   38 39 41 42 43 44 45 46   01234567  89ABCDEF
```

REG and REGBRK Commands

REG Command. The REG command is used to examine and optionally, to modify the internal registers of the 8048/49/21/41A microprocessor. The syntax of the REG command is:

REG [parameter]

where parameter entry is defined in the list which follows:

The following list describes standard register names, flags, response values, and other conditions associated with the parameter when the REG or REGBRK command is issued. The effectivity for REG and/or REGBRK is indicated by an X in their respective columns. The availability of registers in specific 8048 Family groups is indicated by an X in their respective columns.

LIST OF PARAMETERS FOR REG AND REGBRK COMMAND

PARAMETER	GROUP AVAILABILITY 48/49	21	41A	EFFECTIVITY REG	REG BRK	DESCRIPTION	ALLOWED VALUE
	X						
A	X	X	X	X	X	Accumulator	HEX BYTE
C	X	X	X	X	X	Carry Flag	0, 1
AC	X	X	X	X	X	Auxiliary Carry Flag	0, 1
F0	X		X	X	X	Flag 0	0, 1
F1	X		X	X	X	Flag 1	0, 1
TF	X	X	X	X	X	Timer Flag	0, 1
TCR	X	X	X	X	X	Timer/Counter Register	HEX BYTE
SP	X	X	X	X	X	Stack Pointer	0-7, or 8-16 HEX
RB	X		X	X	X	Register Bank	0, 1
R0	X	X	X	X	X	Register 0	HEX BYTE
R1	X	X	X	X	X	Register 1	HEX BYTE
R2	X	X	X	X	X	Register 2	HEX BYTE
R3	X	X	X	X	X	Register 3	HEX BYTE
R4	X	X	X	X	X	Register 4	HEX BYTE
R5	X	X	X	X	X	Register 5	HEX BYTE
R6	X	X	X	X	X	Register 6	HEX BYTE
R7	X	X	X	X	X	Register 7	HEX BYTE
PC	X	X	X		X	Program Counter	ADDRESS
IIP*	X		X		X	Interrupt in Progress	Y(Yes), N(No)
EI*	X		X	X	X	Enable Interrupts	E(Enable), D(Disable)
TI*	X		X	X	X	Enable timer Interrupt	E(Enable), D(Disable)
TCS*	X	X	X	X	X	Timer Counter State	STOP, TIMR, CNTR
MB*	X			X	X	Memory Bank	0, 1
IBF*			X		X	Input Buffer Full	0, 1
OBF*			X		X	Output Buffer Full	0, 1
STS*			X		X	Status (special 4 bits for 8041A)	HEX NIBBLE
ENF*			X		X	Enable Flags	Y(Yes), N(No)
END*			X		X	Enable DMA	Y(Yes), N(No)

NOTE: * indicates special information maintained by the emulator. This information goes beyond the documented hardware registers and flags of an 8048 Family CPU.

REG, REGBRK (Continued)

REGBRK Command. The REGB)rk command is used to define a register breakpoint as determined by one to eight breakpoint test conditions involving specific registers. The break occurs only when all conditions are true. The emulator operates in a SINGLE STEP MODE whenever a REGBRK condition has been established. The syntax of the REGB)rk command is:

REGB)rk [clear] [condition 1... [condition 8]...]

where parameters for:

Clear = Clear current conditions. If this parameter is not specified, any new conditions, 1...8 will be appended to the existing breakpoint conditions.

Condition = The parameters for conditions 1 through 8 are associated with the Register-Relations value that is specified with the register name to establish when or where the break is to occur. If no parameters are specified, the current register breakpoint conditions are displayed.

For all registers, the relation values are shown below. Note that a period is used as a delimiter in front of, and after the specified value.

REGISTER RELATION VALUE	DESCRIPTION
.EQ.	Equal
.NE.	Not equal
.LT.	Two's complement - Less Than
.ULT.	Unsigned - Less Than
.GT.	Two's complement - Less Than
.UGT.	Unsigned - Greater Than
.LE.	Two's complement - Less Than or Equal
.ULE.	Unsigned - Less Than or Equal
.GE.	Two's complement - Greater Than or Equal
.UGE.	Unsigned - Greater Than or Equal

REG, REGBRK (Continued)

Since the same register name can appear in more than one break condition, a range of values can be established. For example, the entry of register name, PCNEXT and register relation value, .UGE. is entered as follows:

```
REGBRK          PC.UGE.100 PC.ULE.1FF
```

This command entry will cause a break to occur whenever the Program Counter is positioned between the range of 100 and 1FF

DRT Command

The DR)t command displays data captured in the real time trace buffer. The hexadecimal opcode is disassembled for bytes of instruction fetches and the mnemonic opcode is presented in the display. The following example shows the 8048/49/21/41A format for the trace buffer display.

```
D>DR)t
  LOC   DATA    BUS    7 CLIPS 0       INSTRUCTION                DATA

  0026   90     MRF    0000 0000       MOVX  @R0,A                 00
  1030   00     MW     0000 0000
  0027   18     MRF    0000 0000       INC   R0
  0028   EA     MRF    0000 0000       DJNZ  R2,0024
  0029   24     MR     0000 0000
  0024   F0     MRF    0000 0000       MOV   A,@R0
  0025   E3     MRF    0000 0000       MOVP3 A,@A                 01
  0331   01     MR     0000 0000
  0026   90     MRF    0000 0000       MOVX  @R0,A                01
  1031   01     MW     0000 0000
  0027   18     MRF    0000 0000       INC   R0
  0028   EA     MRF    0000 0000       DJNZ  R2,0024
  0029   24     MR     0000 0000
  0024   F0     MRF    0000 0000       MOV   A,@R0
    .
    .
    .
    .
  0024   F0     MRF    0000 0000       MOV   A,@R0
  0025   E3     MRF    0000 0000       MOVP3 A,@A                 0F
  0346   0F     MR     0000 0000
  0026   90     MRF    0000 0000       MOVX  @R0,A                0F
  103F   0F     MW     0000 0000
  0027   18     MRF    0000 0000       INC   R0
  0028   EA     MRF    0000 0000       DJNZ  R2,0024
  0029   24     MR     0000 0000
  002A   04     MRF    0000 0000       JMP   002A
  002B   2A     MR     0000 0000
```

At this time it might be desirable for the user to use the DD)ata command to display External Data results as follows:

```
DD)ata X 30 3A
   Addr 0  1  2  3  4  5  6  7   8  9  A  B  C  D  E  F    ASCII
EXT 30=00 01 02 03 04 05 06 07  08 09 0A 0B 0C 0D 0E 0F   ........  ........
D>
```

Refer to note on page 3-7 for value of Memory Bank Flag.

STATUS Command

The S)tatus command is used to query and display the current status of the emulator test environment and CPU dependent register and test conditions for the 8048/49/21/41A microprocessor.

The syntax of the STATUS command is:

S)tatus [parameter]

where the parameter entry is one of the following:

E)nv - Display only the emulation test environment information

R)eg - Display only the CPU dependent register information

If no parameter is specified, the system will display both the emulator test environment and the CPU dependent register information.

The emulation test environment information is standard regardless of the microprocessor type and includes the following testing conditions:

- o Name of Processor version
- o Bias Setting
- o Counter Selection and Value
- o Event Definitions
- o Mapping Information
- o Realtime Trace Qualification
- o Trigger and Breakpoint Definitions
- o Register Break Definition
- o Emulator State:
  - --Paused
  - --Halted
  - --Faulted
  - --Address Specified in Go Encountered
  - --Single Cycle Completed
  - --Memory Write Failure

The 8048/49/21/41A CPU dependent test conditions consist of data, flags and test criteria as defined in subsequent parameters.

The information displayed for the STATUS REG command is formatted as follows:

```
LOC  MNEM  OPRD/EADDR   A  C AC F01 TF TCR SP RB R0 R1 R2 R3 R4 R5 R6 R7 PCNEXT
0011 ORL   A,@R0       CC  0  0  00  0  00 08  0 00 00 00 00 00 00 00 00   0012
           00                                   1 00 00 00 00 00 00 00 00

IIP EI TI   TCS  MB   RETURN
 N   D  D  STOP   0  1100 8FF
```

STATUS (Continued)

The effective address is displayed whenever indexed addressing is used or when the instruction contains a 16-bit immediate value. The latter case is included so that the immediate value is displayed as both an absolute number and a relative address, since either form may be relevant to the user.

The processor status flags in the Trace Line are presented as bits and are individually labeled. The information presented in the various data fields of the display presents the following status conditions. The allowed values for each data field are described in the List of Parameters for REG and REGBRK command.

DESCRIPTION OF DATA FIELDS DISPLAYED FOR STATUS REG COMMAND

MNEMONIC	DESCRIPTION
LOC	-- Address of the last instruction executed.
MNEM	-- Instruction Mnemonic.
OPRD/EADDR	-- First line is the Operand of the last instruction executed, the second line is the Effective Address (displayed when indexed addressing is used or when instruction contains a 16-bit immediate value).

The descriptions of Flags and Registers A through R7 and IIP through MB are the same as those used in the REG command.

PCNEXT	-- Address of the next instruction fetch.
RETURN	-- The contents of the last entry on the stack. If a return instruction is encountered, the PC will be restored. For a RETR instruction, both PC and PSW will be restored.

PORT COMMAND

The P)ort command is used to read from, and write to a port. No check is made after the data is written. In addition, the read or write operation can be updated until terminated by an ESCAPE.

COMMAND SYNTAX

P)ort addr [hh] [Rep]

where:

addr = Valid port address for the 8048/49/21/41A. Ports are 0, 1, 2, 4, 5, 6, or 7.

nn = Hexadecimal Data. If this parameter is used, the data hh is written to the port. If this parameter is omitted, a read from the port occurs.

rep = Repeat parameter which causes the emulator to repeat the read or write operation until the user aborts the process with an ESCAPE.

A typical display for the P)ort command is presented in the following example:

```
D>P)ort 1 87
D>P)ort 1
0001=87
D>
```

RESET Command

When this command is given, a reset signal is applied to the reset pin on the processor, and PCNEXT is set to 0. The following registers and flags are also reset:

- Sets stack pointer to 0
- Selects RB0
- Selects MB0 (8048 Group)
- Sets Bus to a high impedance state (except when EA=5V)
- Sets Ports 1 and 2 to input mode
- Disable interrupts (timer and external)
- Stops timer
- Clears timer flag
- Clears F0 and F1 (8048 and 8041A Groups)
- Disables clock output from T0

For the 8041A Group, the following additional registers and flags are reset:

- Input Buffer Full
- Output Buffer Full
- Status ST7-ST4
- EN Flags
- EN DMA

OPERATION

GENERAL

The 9508 MicroSystem Emulator Manual describes all system commands and includes general operating procedures for the system. This chapter describes unique system operations for the 8048/49/21/41A Emulator Option as related to the design characteristics of the 8048/49/21/41A microprocessor chip.

The 8048/49/21/41A emulator hardware components must have been installed, connected and checked out for emulation as described in chapter 2. Operation of the 8048/49/21/41A Emulator Option involves the following types of user activity:

- o Initializing the emulator system
- o Downloading the users program from host computer system to the emulator system via the communications link
- o Display microprocessor status and modify the contents of internal CPU registers using the STATUS and REG commands
- o Select and alter CPU registers and flags using the REG command
- o Examine and modify CPU instructions in memory by using the DISM and ASM command
- o Control execution using the GO command.
- o Set register breakpoint and display the trace buffer contents using the REGBRK and DRT commands
- o Uploading the debugged program from the emulator to the host computer system via the communications link

INITIALIZATION

The 9508 system can be initialized from a cold start by operating the POWER switch or by restarting system operations with the RESET switch. Refer to the Installation and Checkout Procedure in chapter 3 of the 9508 MicroSystem Emulator manual. This manual describes the 9508 self test diagnostic, system initialization and error conditions associated with the start up. Use the following procedure to power up the system from a cold start:

1. Turn on the POWER switch at the display terminal.

   a. On the 9501 Terminal, a bell will beep within 1 second to indicate power is on.

   b. After a few seconds, the cursor will appear in the upper left-hand corner of the screen. At this time, the operator can adjust the contrast to obtain the desired brilliance for the screen.

2. Turn on the POWER switch at the 9508 MicroSystem Emulator.

   a. The system will perform a self test and initialization process. If no errors are present during start up, a message is displayed ending with the prompt character as shown in the 8048/49/21/41A Emulator Start Up Message example below.

   b. If an error condition is encountered during start up, the following message is displayed:

      ** System Error xx **

      where: xx is an error code number that is described in chapter 3 of the 9508 MicroSystem Emulator Manual.

8048/49/21/41A EMULATOR START UP MESSAGE

```
9508 READY VER X.X   (Where X.X = Software revision level)

PROCESSOR=8048 VX.X
W=0000 X=0000 Y=0000 Z=0000
MAPPED  RAM 1 START=0000  END=1FFFF
EVent Address  Data  Bus   7 CLIPS 0 TRig Pass cnt   Delay cnt    TMode  SEL TRIG
  1   = OFF   =OFF   All   XXXX XXXX  1      0 E1        0 MS  T1 IND        T1
  2   = OFF   =OFF   All   XXXX XXXX  2      0 E2        0 MS  T2 IND        T2

BReak T1=Dsbl  T2=Dsbl    Count=    0 MS    Qual=ALL
  LOC  MNEM  OPRD/EADDR  A C AC F01 TF TCR SP RB R0 R1 R2 R3 R4 R5 R6 R7 PCNEXT
  0011 ORL   A,@R0      CC 0  0  00  0  00 08  0 00 00 00 00 00 00 00 00   0012
             00                                1 00 00 00 00 00 00 00 00

IIP EI TI   TCS  MB   RETURN
 N   D  D  STOP   0  1100 8FF
REGBRK CONDITIONS:

SYSTEM MODE
```

The emulator start up message contains 15 lines of information which presents the standard emulator test environment (lines 1-8) and CPU dependent test conditions (lines 9-15).

The abbreviations used for the standard emulator test environment (lines 1-8) are described in chapter 8 of the 9508 MicroSystem Users Manual which defines the content displayed for each line of information.

The abbreviations used for the 8048/49/21/41A CPU dependent test conditions (lines 9-15) are described in chapter 3 of this addendum (see description of STATUS REG command).

DOWNLOADING USERS PROGRAM FROM HOST

Details of intersystem communication for downloading and uploading data between the emulator and host system is described in chapter 6 of the 9508 MicroSystem Emulator Manual. Refer to this information which presents procedures for the following coverage.

- Communication Link Protocol (Electrical, ACK/NAK, None)
- Data Block Characteristics (TEKHEX, Binary Formats)
- Channel Characteristics (Half/Full Duplex; Parity Designation, None, odd, even, Baud Rate)
- Details of Message Block Formats
- Use of RHEX/WHEX commands for upload/download operation with description of defaults and error conditions

After the download operation is completed, the communications link can be disconnected from the host system and the emulation processing can be conducted at the emulator in a stand-alone mode.

CONFIGURING EMULATION TEST ENVIRONMENT

The emulation test environment can be established after the users program is downloaded from the host. Set up of the emulation test environment involves the use of various commands to select test conditions for the 8048/49/21/41A target system microprocessor. The Start Up Message display, described in previous sections for Initialization, contains 15 lines of information that must be specified by the user for the following emulation test conditions:

- Setting of Bias Registers, W, X, Y, and Z.

- Control Settings for Event, Data Bus, Trace Clips, Triggers, Pass Count, Delay Count, etc.
- Break and Trace Conditions for Trigger Setting Counter and type of data to be collected.
- Specific conditions for the 8048/49/21/41A microprocessor to be emulated (i.e., registers, flags, interrupts, program counter, etc.).
- Register Breakpoint Conditions.
- Emulator Operating Mode for either System Mode (S) where the processor clock is supplied by the emulator with mapped memory used for emulation, or User Mode (U) where the processor clock is supplied by the UUT and resident memory is either at the UUT source or mapped by the emulator.

After the test environment is configured by the user, the status of the test conditions can be displayed by entering the S)tatus command. The various commands for setting the test conditions and parameters are described in chapter 5 of the 9508 MicroSystem Emulator Manual.

The established configuration of the emulation test environment remains available for use until it is either changed by the user, or when the system is reset or powered down.

BREAKPOINT AND TRACE LINES

The GO command is used to begin execution at a specified address. The mode of execution for continuous run, single step, etc. is as specified in the command along with break and trace requirements. Breakpoint and trace lines appear on the display as a result of conditions specified in the GO command. These conditions include instruction fetches encountering, event comparisons, machine status, and CPU timing conditions. Addresses and data are displayed in hexadecimal format. Instructions are displayed in the 8048/49/21/41A Instruction Mnemonic Format. (See appendix C.)

The trace line display format is as follows:

```
D>GO 20 UNTIL 2A TRACE ALL
  LOC  MNEM   OPRD/EADDR A C AC F01 TF TCR SP RB R0 R1 R2 R3 R4 R5 R6 R7 PCNEXT
  0020 MOV    R2,#10     CC 0  0  00  0  00 08  0 00 00 10 00 00 00 00 00   0022
                                                 1 00 00 00 00 00 00 00 00
  0022 MOV    R0,#30     CC 0  0  00  0  00 08  0 30 00 10 00 00 00 00 00   0024
                                                 1 00 00 00 00 00 00 00 00
  0024 MOV    A,@R0      30 0  0  00  0  00 08  0 30 00 10 00 00 00 00 00   0025
               00                                1 00 00 00 00 00 00 00 00
  0025 MOVP3  A,@A       00 0  0  00  0  00 08  0 30 00 10 00 00 00 00 00   0026
                                                 1 00 00 00 00 00 00 00 00
  0026 MOVX   @R0,A      00 0  0  00  0  00 08  0 30 00 10 00 00 00 00 00   0027
               00                                1 00 00 00 00 00 00 00 00
  0027 INC    R0         00 0  0  00  0  00 08  0 31 00 10 00 00 00 00 00   0028
                                                 1 00 00 00 00 00 00 00 00
  0028 DJNZ   R2,0024    00 0  0  00  0  00 08  0 31 00 0F 00 00 00 00 00   0024
                                                 1 00 00 00 00 00 00 00 00
  0024 MOV    A,@R0      31 0  0  00  0  00 08  0 31 00 0F 00 00 00 00 00   0025
               00                                1 00 00 00 00 00 00 00 00
  0025 MOVP3  A,@A       01 0  0  00  0  00 08  0 31 00 0F 00 00 00 00 00   0026
                                                 1 00 00 00 00 00 00 00 00
  0026 MOVX   @R0,A      01 0  0  00  0  00 08  0 31 00 0F 00 00 00 00 00   0027
               00                                1 00 00 00 00 00 00 00 00
    .
    .
    .
  0024 MOV    A,@R0      46 0  0  00  0  00 08  0 3F 00 01 00 00 00 00 00   0025
               00                                1 00 00 00 00 00 00 00 00
  0025 MOVP3  A,@A       0F 0  0  00  0  00 08  0 3F 00 01 00 00 00 00 00   0026
                                                 1 00 00 00 00 00 00 00 00
  0026 MOVX   @R0,A      0F 0  0  00  0  00 08  0 3F 00 01 00 00 00 00 00   0027
               00                                1 00 00 00 00 00 00 00 00
  0027 INC    R0         0F 0  0  00  0  00 08  0 40 00 01 00 00 00 00 00   0028
                                                 1 00 00 00 00 00 00 00 00
  0028 DJNZ   R2,0024    0F 0  0  00  0  00 08  0 40 00 00 00 00 00 00 00   002A
                                                 1 00 00 00 00 00 00 00 00
  LOC  MNEM   OPRD/EADDR A C AC F01 TF TCR SP RB R0 R1 R2 R3 R4 R5 R6 R7 PCNEXT
  002A JMP    002A       0F 0  0  00  0  00 08  0 40 00 00 00 00 00 00 00   002A
                                                 1 00 00 00 00 00 00 00 00
UNTIL BREAK POINT
EMULATION STOPPED
```

where: The processor status flags in the trace line are presented as bits and are individually labeled. The following information is presented in the trace line.

OPERATION

LOC -- Address of the last instruction executed.

MNEM -- Instruction Mnemonic

OPRD/EADDR -- First line is the Operand of the last instruction executed, the second line is the Effective Address (displayed when indexed addressing is used or when instruction contains a 16-bit immediate value).

A -- Accumulator

C -- Carry Falg

AC -- Auxillary Carry Flag

F01 -- Flags 0 and 1, respectively

TF -- Timer Flag

TCR -- Timer/Counter Register

SP -- Stack Pointer

RB -- Register Bank

R0-R7 -- Registers 0 through 7

PCNEXT -- Address of the next instruction fetch.

The contents of the trace buffer are displayed on the screen, twenty-two lines at a time along with a format line.

AC CHARACTERISTICS

Table A-1. 8048/8035 AC Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V

Symbol	Parameter	8048 8648 8748/8035/8035L			8748-8 8035-8			Unit	Conditions
		Min.	Max.	Diff.	Min.	Max.	Diff.		
t_{LL}	ALE Pulse Width	400		0	600		0	ns	
t_{AL}	Address Setup to ALE	150		0	150		0	ns	
t_{LA}	Address Hold from ALE	80		0	80		0	ns	
t_{CC}	Control Pulse Width (PSEN, RD, WR)	700		0	1500		0	ns	
t_{DW}	Data Setup before $\overline{WR}$	500		0	640		0	ns	
t_{WD}	Data Hold After $\overline{WR}$	120		-15	120		-15	ns	C_L = 20pF
t_{CY}	Cycle Time	2.5	15.0	0	4.17	15.0	0	us	6 MHz XTAL (3.6MHz XTAL for -8)
t_{DR}	Data Hold	0	200	0	0	200	0	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500	0		750	0	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		0	260		0	ns	
t_{AD}	Address Setup to Data In		950	0		1450	0	ns	
t_{AFC}	Address Float to RD, PSEN	0		0	0		0	ns	
t_{CA}	Control Pulse to ALE	10		0	20		0	ns	

Table A-2. 8048/8035 Port 2 AC Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Diff.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of PROG	110		-30	ns	
t_{PC}	Port Control Hold After Falling Edge of PROG	140		0	ns	
t_{PR}	PROG to Time P2 Input Must be Valid		810	-20	ns	
t_{DP}	Output Data Setup Time	220		-20	ns	
t_{PD}	Output Data Hold Time	65		-20	ns	
t_{PF}	Input Data Hold Time	0	150	0	ns	
t_{PP}	$\overline{\text{PROG}}$ Pulse Width	1510		0	ns	
t_{PL}	Port 2 I/O Data Setup	400		0	ns	
t_{LP}	Port 2 I/O Data Hold	150		0	ns	

Table A-3. 8049/8039/8039-6 AC Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V

Symbol	Parameter	8049/8039 (Note 1)			8039-6			Unit	Conditions (Note 2)
		Min.	Max.	Diff.	Min.	Max.	Diff.		
t_{LL}	ALE Pulse Width	150		0	400		0	ns	
t_{AL}	Address Setup to ALE	70		0	150		0	ns	
t_{LA}	Address Hold from ALE	50		0	80		0	ns	
t_{CC}	Control Pulse Width (PSEN, RD, WR)	300		0	700		0	ns	
t_{DW}	Data Set-Up Before WR	250		0	500		0	ns	
t_{WD}	Data Hold After WR	40		-15	120		-15	ns	C_L = 20 pF
t_{CY}	Cycle Time	1.36	15.0	0	2.5	15.0	0	us	11 MHz XTAL (6 MHz XTAL for -6)
t_{DR}	Data Hold	0	100	0	0	200	0	ns	
t_{RD}	PSEN, RD to Data In		200	0		500	0	ns	
t_{AW}	Address Setup to WR	200		0	230		0	ns	
t_{AD}	Address Setup to Data In		400	0		950	0	ns	
t_{AFC}	Address Float to RD, PSEN	-10		0	0		0	ns	

NOTES: 1. 8039-6 specifications are also valid for 8049/8039 operating at 6 MHz.

2. Control Outputs: C_L = 80 pF
   Bus Outputs: C_L = 150 pF

Table A-4. 8049/8039/8039-6 Port 2 AC Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	8049/8039			8039-6			Unit	Conditions (Note 1)
		Min.	Max.	Diff.	Min.	Max.	Diff.		
t_{CP}	Port Control Setup Before Falling Edge of PROG	100		-30	110		-30	ns	
t_{PC}	Port Control Hold After Falling Edge of PROG	60		0	140		0	ns	
t_{PR}	PROG to Time P2 Input Must be Valid		650	-20		810	-20	ns	
t_{DP}	Output Data Setup Time	200		-20	220		-20	ns	
t_{PD}	Output Data Hold Time	20		-20	65		-20	ns	
t_{PF}	Input Data Hold Time	0	150	0	0	150	0	ns	
t_{PP}	PROG Pulse Width	700		0	1510		0	ns	
t_{PL}	Port 2 I/O Data Setup	150		0	400		0	ns	
t_{LP}	Port 2 I/O Data Hold	20		0	150		0	ns	

NOTE: 1. Control Outputs: C_L = 80 pF
Bus Outputs: C_L = 150 pF

Table A-5. 8021 AC Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.5V ± V, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Diff.	Unit	Test Conditions
t_{CY}	Cycle Time	10.0	50.0	0	u sec	3 MHz XTAL = 10 u sec
F	Oscillator Frequency Variation-Resistor Mode	-20	+20	0	%	F = 2.5 MHz

Command and execution errors are displayed at the console terminal. Command errors are indicated by pointing to the error location in the command line and displaying an error code message. The following examples present a typical error message:

```
D > BIES     W=20              ** ERROR FF **
     ^
D > DUMP     30       10       ** ERROR 14 **
                      ^
D > EXAM      4P               ** ERROR 02 **
              ^
```

where: ERROR #FF = INVALID COMMAND

ERROR #14 = LOWER ADDRESS IS NOT LESS THAN OR EQUAL TO UPPER ADDRESS

ERROR #02 = INVALID PARAMETER

Execution errors that occur during emulation processing may also indicate other types of error information.

The complete description of all error conditions that are presented for a given error code number is provided in Appendix A of the 9508 MicroSystem Emulator Manual.

8048/49/21/41A INSTRUCTION SET AND REGISTER INFORMATION

The following pages contain information about the 8048/49/21/41A instruction set and the registers. Any special instructions relative to the 8048/49/21/41A are also included in this appendix.

For all of the following tables, X represents a valid instruction for the microprocessor in whose column the X appears.

Table C-1. Accumulator Instructions

GROUP					HEX OP CODE
8048/49	8021	8041A	MNEMONIC	DESCRIPTION	
X	X	X	ADD A,Rr	Add register to A *	68-6F
X	X	X	ADD A,@Rr	Add data memory to A	60-61
X	X	X	ADD A,#data	Add immediate to A	03
X	X	X	ADDC A,Rr	Add register with carry *	78-7F
X	X	X	ADDC A,@Rr	Add data memory with carry	70-71
X	X	X	ADDC A,#data	Add immediate with carry	13
X	X	X	ANL A,Rr	And register to A *	58-5F
X	X	X	ANL A,@Rr	And data memory to A	50-51
X	X	X	ANL A,#data	And immediate to A	53
X	X	X	ORL A,Rr	Or register to A *	48-4F
X	X	X	ORL A,@Rr	Or data memory to A	40-41
X	X	X	ORL A,#data	Or immediate to A	43
X	X	X	XRL A,Rr	Exclusive or register to A *	D8-DF
X	X	X	XRL A,@Rr	Exclusive or data memory to A	D0-D1
X	X	X	XRL A,#data	Exclusive or immediate to A	D3
X	X	X	INC A	Increment A	17
X	X	X	DEC A	Decrement A	07
X	X	X	CLR A	Clear A	27
X	X	X	CPL A	Complement A	37
X	X	X	DA A	Decimal adjust A	57
X	X	X	SWAP A	Swap nibbles of A	47
X	X	X	RL A	Rotate A left	E7
X	X	X	RLC A	Rotate A left through carry	F7
X	X	X	RR A	Rotate A right	77
X	X	X	RRC A	Rotate A right through carry	67

* = See Table C-10

Table C-2. Input/Output Instructions

GROUP			MNEMONIC	DESCRIPTION		HEX OP CODE
8048/49	8021	8041A				
	X		IN A,Pp	Input port to A		08
X		X	IN A,Pp	Input port to A		09
X			IN A,Pp	Input port to A		0A
X		X	OUTL Pp,A	Output A to port		39,3A
	X		OUTL Pp,A	Output A to port		90
X		X	ANL Pp,#data	And immediate to port		99-9A
X		X	ORL Pp,#data	Or immediate to port		89-8A
X			INS A,BUS	Input BUS to A		08
X			OUTL BUS,A	Output A to BUS		02
X			ANL BUS,#data	And immeidate to BUS		98
X			ORL BUS,#data	Or immediate to BUS		88
X	X	X	MOVD A,Pp	Input expander port to A		0C-0F
X	X	X	MOVD Pp,A	Output A to expander port	**	3C-3F
X	X	X	ANLD Pp,A	And A to expander port	**	9C-9F
X	X	X	ORLD Pp,A	Or A to expander port	**	8C-8F
		X	IN A,DBB	Input DBB to A, clear IBF		22
		X	OUT DBB,A	Output A to DBB, set OBF		02

** = See Table C-11

Table C-3. Register Instructions

GROUP			MNEMONIC	DESCRIPTION		HEX OP CODE
8048/49	8021	8041A				
X	X	X	INC Rr	Increment register	*	18-1F
X	X	X	INC @ Rr	Increment data memory		10-11
X		X	DEC Rr	Decrement register	*	C8-CF

* = See Table C-10

Table C-4. Branch Instructions

GROUP			MNEMONIC	DESCRIPTION	HEX OP CODE
8048/49	8021	8041A			
X	X	X	JMP addr	Jump unconditional †	04,24, 44,64, 84,A4, C4,E4
X	X	X	JMPP @A	Jump indirect	B3
X	X	X	DJNZ R,addr	Decrement register and jump *	E8-EF
X	X	X	JC addr	Jump on Carry = 1	F6
X	X	X	JNC addr	Jump on Carry = 0	E6
X	X	X	JZ addr	Jump on A Zero	C6
X	X	X	JNZ addr	Jump on A not Zero	96
X		X	JT0 addr	Jump on T0 = 1	36
X		X	JNT0 addr	Jump on T0 = 0	26
X	X	X	JT1 addr	Jump on T1 = 1	56
X	X	X	JNT1 addr	Jump on T1 = 0	46
X		X	JF0 addr	Jump on F0 = 1	B6
X		X	JF1 addr	Jump on F1 = 1	76
X	X	X	JTF addr	Jump on timer flag = 1	16
X			JNI addr	Jump on $\overline{INT}$ = 0	86
X		X	JBb addr	Jump on Accumulator bit	12,32, 52,72, 92,B2, D2,F2
		X	JNIBF addr	Jump on IBF Flag = 0	D6
		X	JOBF addr	Jump on OBF Flag = 1	86

* = See Table C-10 † = See Table C-12

Table C-5. Subroutine Instructions

GROUP			MNEMONIC	DESCRIPTION	HEX OP CODE
8048/49	8021	8041A			
X	X	X	CALL addr	Jump to subroutine †	14,34, 54,74, 94,B4, D4,F4
X	X	X	RET	Return	83
X		X	RETR	Return and restore status	93

† = See Table C-12

Table C-6. Flag Instructions

GROUP			MNEMONIC	DESCRIPTION	HEX OP CODE
8048/49	8021	8041A			
X	X	X	CLR C	Clear Carry	97
X	X	X	CPL C	Complement Carry	A7
X		X	CLR F0	Clear Flag 0	85
X		X	CPL F0	Complement Flag 0	95
X		X	CLR F1	Clear Flag 1	A5
X		X	CPL F1	Complement Flag 1	B5
		X	MOV STA,A	A_4 - A_7 to bits 4-7 of status	90

Table C-7. Data Move Instructions

GROUP			MNEMONIC	DESCRIPTION	HEX OP CODE
8048/49	8021	8041A			
X	X	X	MOV A,Rr	Move register to A *	F8-FF
X	X	X	MOV A,@Rr	Move data memory to A *	F0-F1
X	X	X	MOV A,#data	Move immediate to A	23
X	X	X	MOV Rr,A	Move A to register *	A8-AF
X	X	X	MOV @Rr,A	Move A to data memory	A0-A1
X	X	X	MOV Rr,#data	Move immediate to register	B8-BF
X	X	X	MOV @Rr,#data	Move immeditae to data memory	B0-B1
X		X	MOV A,PSW	Move PSW to A	C7
X		X	MOV PSW,A	Move A to PSW	D7
X	X	X	XCH A,Rr	Exchange A and register *	28-2F
X	X	X	XCH A,@Rr	Exhange A and data memory	20-21
X	X	X	XCHD A,@Rr	Exchange nibble of A and register	30-31
X			MOVX A,@Rr	Move external data memory to A	80-81
X			MOVX @R,A	Move A to external data memory	90-91
X	X	X	MOVP A,@A	Move to A from current page	A3
X		X	MOVP3 A,@A	Move to A from Page 3	E3

* = See Table C-10

Table C-8. Timer/Counter Instructions

GROUP			MNEMONIC	DESCRIPTION	HEX OP CODE
8048/49	8021	8041A			
X	X	X	MOV A,T	Read Timer/Counter	42
X	X	X	MOV T,A	Load Timer/Counter	62
X	X	X	STRT T	Start Timer	55
X	X	X	STRT CNT	Start Counter	45
X	X	X	STOP TCNT	Stop Timer/Counter	65
X		X	EN TCNTI	Enable Timer/Counter Interrupt	25
X		X	DIS TCNTI	Disable Timer/Counter Interrupt	35

Table C-9. Control Instructions

GROUP			MNEMONIC	DESCRIPTION	HEX OP CODE
8048/49	8021	8041A			
X		X	EN I	Enable external interrupt	05
X		X	DIS I	Disable external interrupt	15
X		X	SEL RB0	Select register bank 0	C5
X		X	SEL RB1	Select register bank 1	D5
X			SEL MB0	Select memory bank 0	E5
X			SEL MB1	Select memory bank 1	F5
X			ENT0 CLK	Enable clock output on T0	75
		X	EN DMA	Enable DMA handshake lines	E5
		X	EN FLAGS	Enable master interrupts	F5
X	X	X	NOP	No operation	00

Table C-10. Register Accumulator

Rr	MOV A,R	MOV R,A	XCH A,R	MOV R, #DATA	INC R	DEC R
R0	F8	A8	28	B8	18	C8
R1	F9	A9	29	B9	19	C9
R2	FA	AA	2A	BA	1A	CA
R3	FB	AB	2B	BB	1B	CB
R4	FC	AC	2C	BC	1C	CC
R5	FD	AD	2D	BD	1D	CD
R6	FE	AE	2E	BE	1E	CE
R7	FF	AF	2F	BF	1F	CF

Table C-10. Register Accumulator (Cont.)

DJNZ R	ADD A,R	ADDC A,R	ANL A,R	ORL A,R	XRL A,R
E8	68	78	58	48	D8
E9	69	79	59	49	D9
EA	6A	7A	5A	4A	DA
EB	6B	7B	5B	4B	DB
EC	6C	7C	5C	4C	DC
ED	6D	7D	5D	4D	DD
EE	6E	7E	5E	4E	DE
EF	6F	7F	5F	4F	DF

Table C-11 INPUT/OUTPUT.

Port	IN	OUT	AND	OR
BUS	08	02	98	88
P1	09	39	99	89
P2	0A	3A	9A	8A
P4	0C	3C	9C	8C
P5	0D	3D	9D	8D
P6	0E	3E	9E	8E
P7	0F	3F	9F	8F

Table C-12 BRANCH

Page	JMP	CALL
0	04	14
1	24	34
2	44	54
3	64	74
4	84	94
5	A4	B4
6	C4	D4
7	E4	F4

Page = 256 bytes

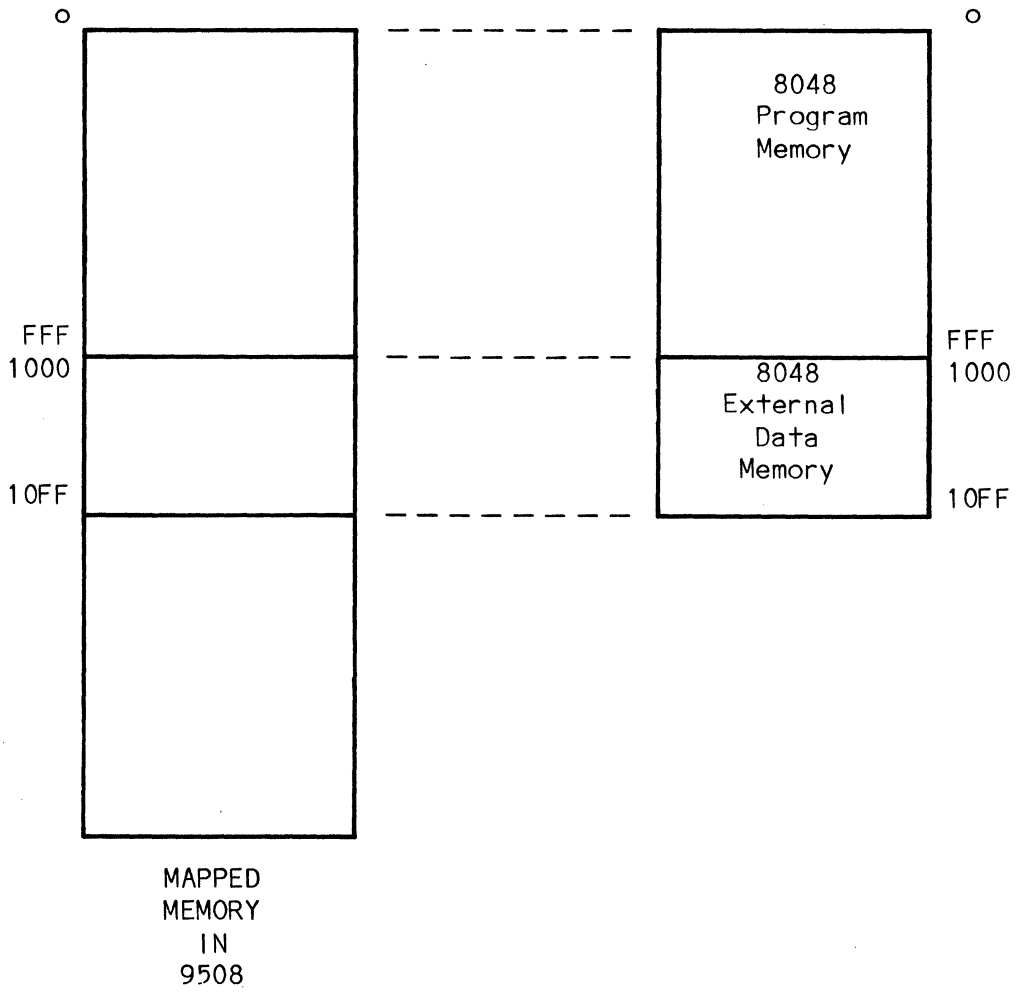


Figure D-1. Memory Map

In the 9508,

```
MAP 1 0 4
```

will substitute 9508 memory for the UUT's Program Memory. Note that the ASM command cannot be used to alter memory which is mapped to the UUT.

```
MAP 1 1000 1
```

will substitute 9508 memory for the UUT's External Data Memory. Accessing External Data Memory will cause addresses in the range 1000-10FF to appear in the Real Time Trace Buffer.

```
MAP 1 0 8
```

will substitute 9508 memory for both Program Memory and External Data Memory.

ORDERING INFORMATION

The 8048/49/21/41A Emulator Option for the 9508 MicroSystem Emulator is ordered by the following order number:

Order Name	Description	Price
XE8048	8048/49/21/41A In-circuit Emulator Option for the 9508 MicroSystem Emulator	See current price list

The Emulator Option parts are listed in Table E-1. The parts may be ordered separately, directly from Millennium or from the Millennium sales office or distributor serving your locality. See the current price list for the price of each item.

Table E-1. Emulator Option Parts List

Part Number	Description
13000125	8048 Family Emulator printed circuit board assembly
15000148	8048/49/21 Emulator Pod assembly
15000178	8041A Emulator Pod assembly
15000147	8048/49/41A Emulator Probe
15000179	8021 Emulator Probe
13000236-03	8048 Family Emulator Dependent PROM printed printed circuit board assembly
87000077	9508 MicroSystem Emulator Users Manual, Addendum for 8048/49/21/41A Emulator Option

Table E-2 lists the sources of accessory equipment for the emulator option.

Table E-2. Accessory Equipment Sources

Equipment	Source	Vendor Part Number
40-Pin header, male/male	Augat	640-AG1
40-Pin header, male/female	Augat	540-AG10D

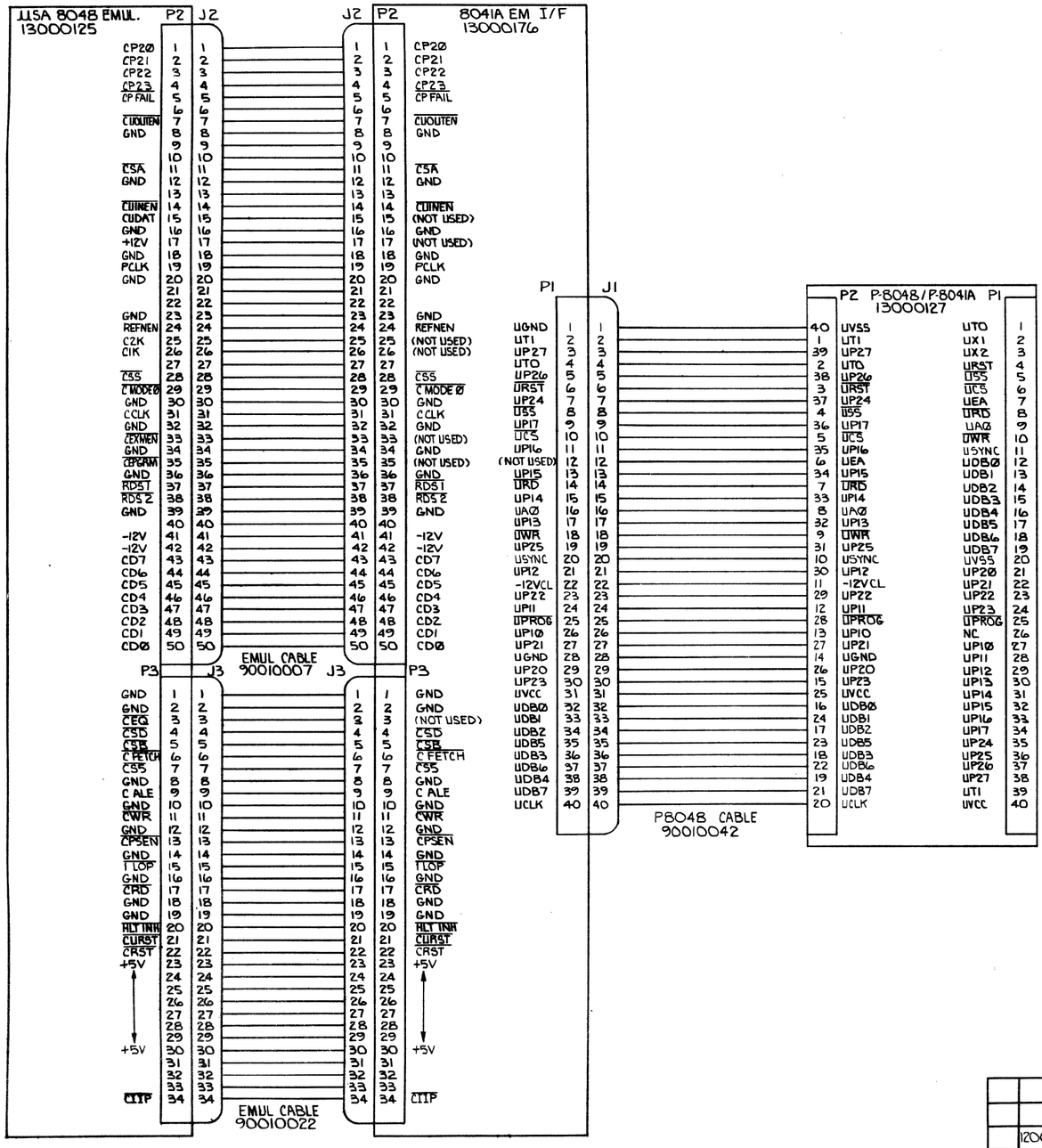
SCHEMATICS

This appendix contains schematic diagrams for the latest revisions of the 8048/49/21/41A Emulator Board, 8048/49/21 and 8041A Emulation Pods, and the 8048/49/41A and 8021 Emulator Probes available at the time the manual was printed. These schematics are subject to change therefore, they are only reference documents.

DWG. NO.	SH	REV.
12000187	1	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	02	ENG. RELEASE	3-10-80	GF
	50	PILOT RELEASE PER ECO 1962	3-20-80	GF
	A	PRODUCTION RELEASE PER ECO 2035	4-30-80	GF



-02	-01	QTY PER ASSY	PART NUMBER	DESCRIPTION	ITEM NO.

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
	12000178	J1SA 8041A

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN T.TAKEDA	1-28-80
CHECKED GF	3-20-80
ENGR GF	3-20-80

Millennium Systems Inc.

J1SA 8041A
WIRING SCHEMATIC

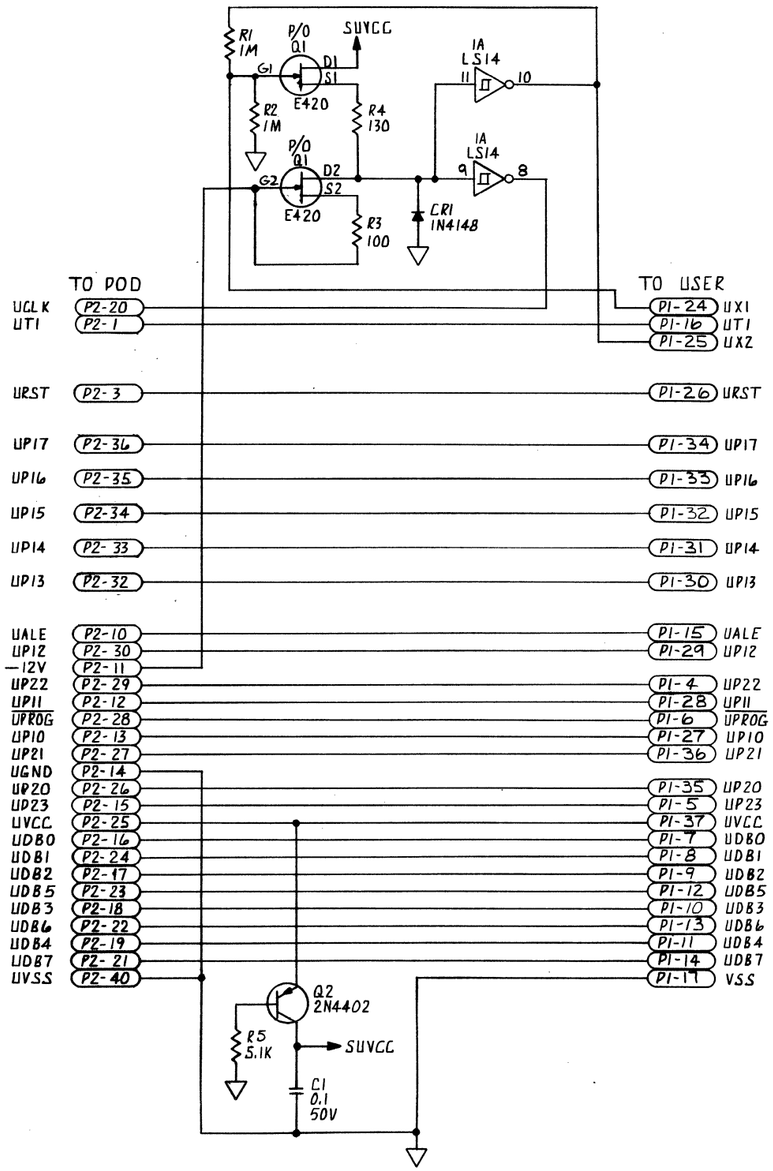
SIZE	DWG. NO.	REV.
D	12000187	A

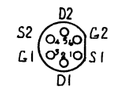
SCALE NONE SHEET 1 OF 1

DWG. NO.	SH	REV.
12000184	1	B

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	50	PILOT RELEASE ECO 1848	1-24-80	CGL
	A	PRODUCTION RELEASE ECO 1963	3-20-80	
	B	PER ECO 1213	12-3-81	





Q1 ORIENTATION
BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS, 1/8W, ±5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.

130001184	8048 USA					
NEXT ASSY	USED ON	LAST USED	NOT USED	TYPE	REF DES	QTY
FIRST APPLICATION		REF DESIGNATIONS		SPARE GATES		

Millennium Systems Inc.

APPROVALS	DATE
DRAWN RHONDA DYER	11-4-79
CHECKED E. STEINERT	11/5/79
ENGR	

SCHEMATIC, USA
8021 PROBE

SIZE D | DWG. NO. 12000184 | REV. B

SCALE: NONE | SHEET 1 OF 1

DWG. NO.	SH	REV.
12000176	1	E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	04	ENG. RELEASE	3-18-80	ET
	50	PILOT RELEASE PER ECO 1962	3-20-80	CJL
	A	PRODUCTION RELEASE PER ECO 2035	4-30-80	CJL
	B	PER ECO 2436	2-19-81	ACZ
	C	PER ECO # 2528	4-23-81	
	D	PER ECO 2623	8-21-81	
	E	PER ECO 2743	9-16-81	ACZ

UTØ (P1-4)

(2D2) DBB IN

(2C2) DBB ØUT

(3C1) BPSEN

UWR (P1-18)

UAØ (P1-16)

URD (P1-14)

UCS (P1-10)

(2C2) ACK

(2B2) FØ FLG

(3A1) 01-05

FIRST CYCLE DECØDER

CUØUTEN (P2-7)

(3A2) PRØG ØUT

(3A2) PRØG IN

CRST (P3-22)

CSA (P2-11)

VCC (P3-23-30)

GND (P2-8, P2-12, P2-16, P2-18, P2-20, P2-23, P2-30, P2-32, P2-34, P2-36, P2-39, P3-1, P3-2, P3-8, P3-10, P3-12, P3-14, P3-16, P3-18, P3-19)

.1 50V UNCODED

C1 47 25V

P1-28, P1-1 U GND

-12V (P2-41, P2-42)

R4 1K

P1-22 -12 VCL

MRD (2B7)

IBF (4A8)

IBF (4D8)

MRRDB (4A8)

ØBF (4A8)

CPLFØ (2B7)

MRRDSTS (4A8)

MUX TØ (3D7)

CLRFØ (2B7)

FI (4A8)

MWR (2B7)(4A8)

EN FLG (2C7)

EN DMA (2C7)

CUØUTEN (2C8)

P2LTHEN (4C8)

STSEN (4A8)

PRØG (4C8)

BCRST (2C7) (4C8)(3D7)

ØUTPZ (4D8)

CRST (4D8)

RETR (2B7)

CSA (4C8)

CSAB (2B7)

NØTES: UNLESS ØTHERWISE SPECIFIED-

1. RESISTØR VALUES ARE IN ØHMS 1/4 W, 5%.
2. CAPACITØR VALUES ARE IN MICRØ-FARADS.
3. SYMBØL ⊐ IS A 10K CØMMØN PULL-UP RESISTØR.
4. RESISTØR PACK (RP) VALUES ARE 68 ØHMS.
5. I.C.'S ARE 7400 FAMILY

NEXT ASSY	USED ON	LAST USED	NOT USED	TYPE	REF DES	QTY
				LS109	8E	1
				7406	3A	1
				LS04	2A	1
				LS00	8B	1
				LS00	1D	1
				LS08	9D	1
				LS14	5A	1
				LS10	3E	1
				LS02	1A	3

FIRST APPLICATION | REF DESIGNATIONS | SPARE GATES

APPROVALS	DATE
DRAWN	12-12-79
CHECKED	1-10-80
ENGR	3-20-80

Millennium Systems Inc.

SCHEMATIC

8041A EMULATØR INTERFACE

SIZE D | DWG. NO. 12000176 | REV. E

NØ SCALE | SHEET 1 OF 4

DWG. NO. 12000176	SH 2	REV. B

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHT.1		

RD STAT 1 (P2-37)
RD STAT 2 (P2-38)
(3C2) INCYZ
(3C2) RD + PSEN
(3A2) INPI DBB
(3A2) MOVSTS
(3C2) WR
(3A2) OUT DBB A
(1B3) CLRDLTEN
(1B3) BCRST
(3C2) BPSEN
(1B3) EN FLG
(4C2) P27L
(1B3) EN DMA
(4D1) DACK
(1A3) CSA B
(1B3) MWR
(1D3) MRD
(1A3) RETR
(1C3) CPL FØ
(1C3) CLR FØ
(1B3) FETPSEN
CIIP (P3-34)
(1A3) BCRST
(3D1) DØ-D7
D2

LS510 3E
LS504 3H
LS502 5F
LS500 3F
LS504 9A
LS502 6E
LS504 6D
LS510 8A
LS504 9A
LS109 2E
NC
+5V
LS502 1A
R5 10K
+5V
C2 2200PF
7406
LS109 2E
LS14 A5
LS500 1D
LS504 9A
LS502 6E
LS158 9B
4B 3B 2B 1B 4A 3A 2A 1A
4Y 3Y 2Y 1Y
NC NC
LS504 6D
LS502 6E
LS504 3H
LS500 3F
LS500 3F
LS500 3F
LS510 3E
LS504 6D
LS109 4E
NC
LS109 4E
LS14 4F
LS109 4E
LS109 8E
N.C.
LS109 2F
N.C.
LS109
LS500 8B
LS00

RD STAT 1 (4A8)
RD STAT 2 (3C8)
CPU IN (3C7)
DBB IN (1D8)(4A8)
MOV STS (4C8)
DBB ØUT (4A8)
DBB ØUT (1D8)
EN FLG LTH (4B8)
DACK EN (4D8)
EN DMA LTH (4B8)
ACK (1C8)
DMA CLR (4D8)
FØ (4A8)(1C8)
IBFI (3D7)

Millennium Systems Inc.	SIZE D	FSCM NO.	DWG. NO. 12000176	REV. B
DRAWN Marina Rosario				
ISSUED	SCALE NONE		SHEET 2 OF 4	

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REORDER NO. A-2259

DWG. NO. 12000176	SH. 3	REV. E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHT. 1		

+5V R6 470Ω — LS04 5A 6 — R7 470Ω +5V

(1C3) MUXTØ
(1B3) BCRST
CCLK P2-31 — LS14 5 6 4F — LS02 6 5 4H 4
UT1 P1-2 — LS14 1 2 5A
(2B1) IBFI
CLK — LS02 12 11 4H 13 — LS14 3 4 5A

CMODEØ P2-29 — LS04 9 3H 8 — LS02 8 9 4H 10
UCLK P1-40 — LS14 5 6 5A

(2D2) RD STAT 2 — LS04 5 6 3H — LS02 3 2 4H 1

URST P1-6 — LS14 11 10 4F
CSS P2-28 — LS14 9 8 4F
USS P1-8 — LS14 13 12 4F
+5V — R2 10K
(2D2) CPUIN

CD0 P2-50 — RP12 2 1 CD0
CD1 P2-49 — RP13 2 1 CD1
CD2 P2-48 — RP12 4 3 CD2
CD3 P2-47 — RP13 4 3 CD3
CD4 P2-46 — RP12 6 5 CD4
CD5 P2-45 — RP13 6 5 CD5
CD6 P2-44 — RP12 8 7 CD6
CD7 P2-43 — RP13 8 7 CD7

81LS97 1H: CD0–CD7 → BD0–BD7
81LS97 2H: CD0–CD7 → BD0–BD7
81LS97 3B: BD0–BD7 → D0–D7
81LS97 2B: BD0–BD7 → D0–D7

6349 1B: BD0–BD7 → D0–D7
TRANSLATØR RØM

8035: XTAL2, TO, RST, XTAL1, T1, INT, VDD, VCC, EA, PSEN, ALE, PROG, VSS
P10–P17 → UP10–UP17
P20–P27 → P20–P27
D0–D7 (4A8)(2A8)
P20–P27 (4C8)

UP10 — RP6 8 7 100 — RP6 6 5 100 — P1-26 UP10
UP11 — RP6 4 3 100 — P1-24 UP11
UP12 — RP6 2 1 100 — P1-21 UP12
UP13 — RP2 8 7 100 — P1-17 UP13
UP14 — RP2 6 5 100 — P1-15 UP14
UP15 — RP2 4 3 100 — P1-13 UP15
UP16 — RP2 2 1 100 — P1-11 UP16
UP17 — P1-9 UP17

WR (2D7)

81LS97 5H: WR, RD, PSEN, ALE, PROG
RP14 3 4 — P3-11 CWR
RP14 7 8 — P3-17 CRD
RP11 5 6 — P3-21 CURST
BPSEN (2C7)
RP14 1 2 — P3-9 CALE
RP11 7 8 — P3-20 HLT INH
RP14 5 6 — P3-13 CPSEN
LS02 7H — FETPSEN (4D8)
LS00 6H — INCY2 (2D7)
RD+PSEN (2D7)
LS04 13 12 3H — FETPSEN (2A7)

LS00 13 12 6H 11
LS00 10 9 6H 8
LS04 5 6F — LS02 8 5F 10
81LS97 6A: CLK → P1-25 U PRØG, P2-24 REFNEN, P2-19 P CLK, P1-20 U SYNC
R3
RP7 4 3
RP7 8 7
RP7 6 5 100

+5V — LS74 J 11, 2F, Q 10 NC, CK 12, K 13, R 15, Q 9
CPUOUT
RD+PSEN
LS04 9 6F 4

LS138 1E: A, B, C, G2A, G2B, G1 → Y0–Y7
Y0 NC
Y1 INP2 (4D8)
Y2 INPI DBB (2D7)
Y3 ØUT DBB A (2C7)
Y4 PRØG IN (1B8)(4D8)
Y5 PRØG ØUT (1B8)(4C8)
Y6 MØV ST5 (2D7)
Y7 NC
SECOND CYCLE DECODER

81LS97 1F: BD0–BD7 → D0–D7
82S115: A0–A8, ST, CE1, CE2 → O1–O8
FETPSEN
ILOP
+5V
ICE DECODER

CUINEN P2-14
CFETCH P3-6
LS04 9 6F 8

O1-O5(1C8)
ILOP — LS04 1 3H 2 — RP11 3 4 — P3-15 ILOP

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Millennium Systems Inc.	SIZE D	FSCM NO.	DWG. NO. 12000176	REV. E
DRAWN Marina Rosario				
ISSUED	SCALE NONE		SHEET 3 ØF 4	

DWG. NO. 12000176	SH 4	REV E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHT. 1		

(2C2) DACK EN
(1D3) IBF
(2B2) DMACLR
(1A8) CRST
CSD P3-4
(1A3) OUT P2
(3B2) FETPSEN
(3A2) PROG IN
(3A1) INPZ
CS5 P3-7
CS8 P3-5
(3A1) PROG OUT
(1B3) PROG
(2B3) P2LTHEN
(1A3) CSA
(1B3) BCRST
(32D) P20-P27
(2D2) MOV STS
(2C2) EN FLG LTH
(2C2) EN DMA LTH
(2D2) RD STAT 1
(1B3) STSEN
(2D2) DBB IN
(1B3) MWR
(3D2) D0-D7
(1D3) MRRDB
(2C2) DBB OUT
(1C3) OBF
(1D3) IBF
(2B2) F0
(1C3) F1
(1C3) MRRDSTS
UVCC P1-31

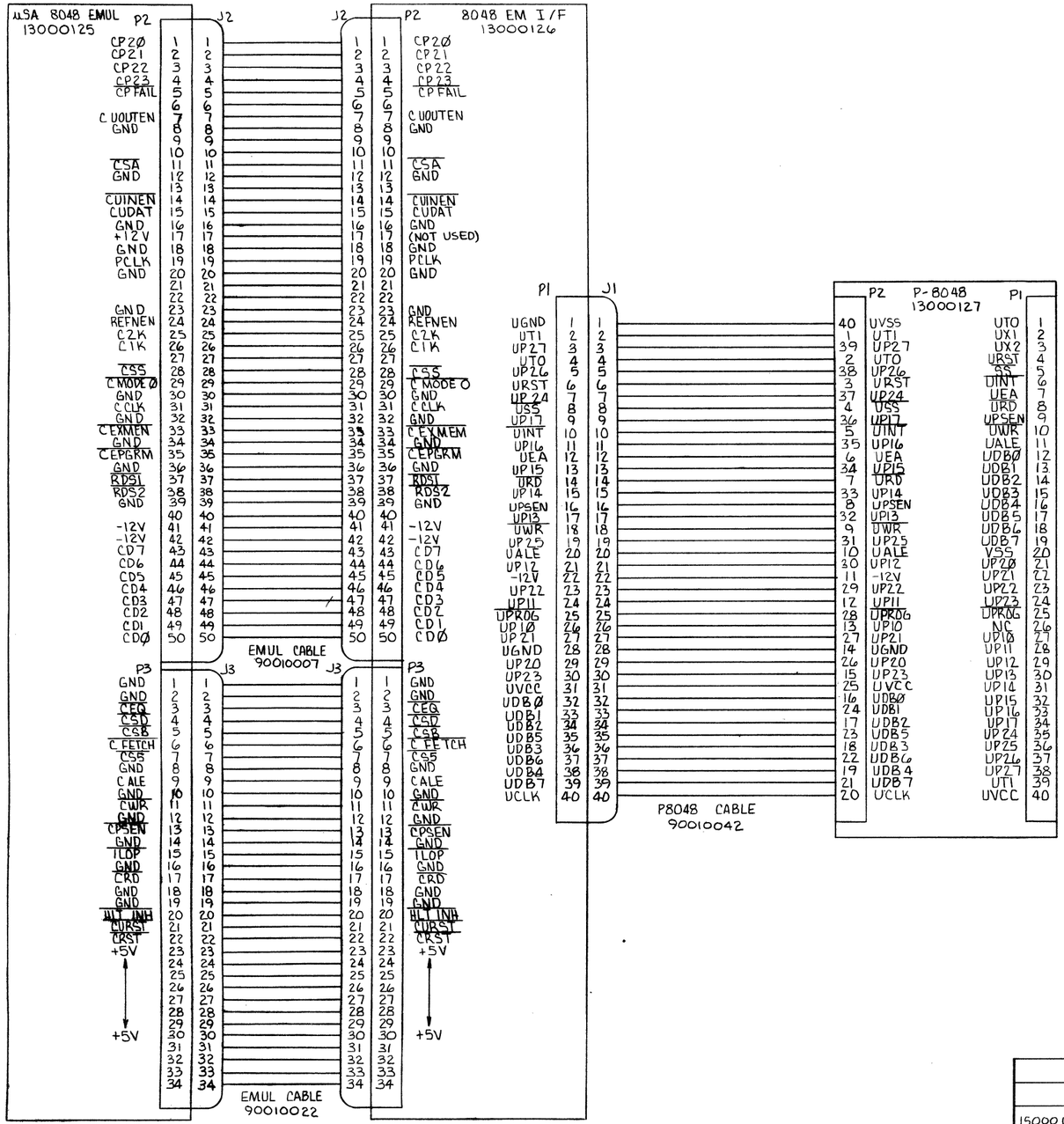
DRQ
P27L
P27L (2C7)
EXP OUT P2
+5V
DACK (2C7)
P1-19 UP25/IBF
P1-3 UP27/DACK
P1-7 UP24/OBF
P1-5 UP26 DRQ
P2-4 CP23
P2-3 CP22
P2-2 CP21
P2-1 CP20
P1-30 UP23
P1-28 UP22
P1-27 UP21
P1-29 UP20
P1-32 UDB0
P1-33 UDB1
P1-34 UDB2
P1-36 UDB3
P1-38 UDB4
P1-35 UDB5
P1-37 UDB6
P1-39 UDB7
P2-5 CP FAIL

Millennium Systems Inc.	SIZE D	FSCM NO.	DWG. NO. 12000176	REV. B
DRAWN Marina Rosario				
ISSUED	SCALE NONE			SHEET 4 OF 4

DWG. NO.	SH	REV.
12000154	1	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	01	PROTO-TYPE		
	02	PROTO TYPE		
	50	PILOT RELEASE ECO #1666	10/15/79	
	51	REVISED PER ECO 1940	2-4-80	
	A	PRODUCTION RELEASE ECO 1963	3-20-80	



QTY. REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

15000146	uSA 8048
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± | DECIMALS .XX ± .XXX ± | ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. SENA	8-27-79
CHECKED	9/18/79
ISSUED	10/12/79

Millennium Systems Inc.

USA 8048
WIRING SCHEMATIC

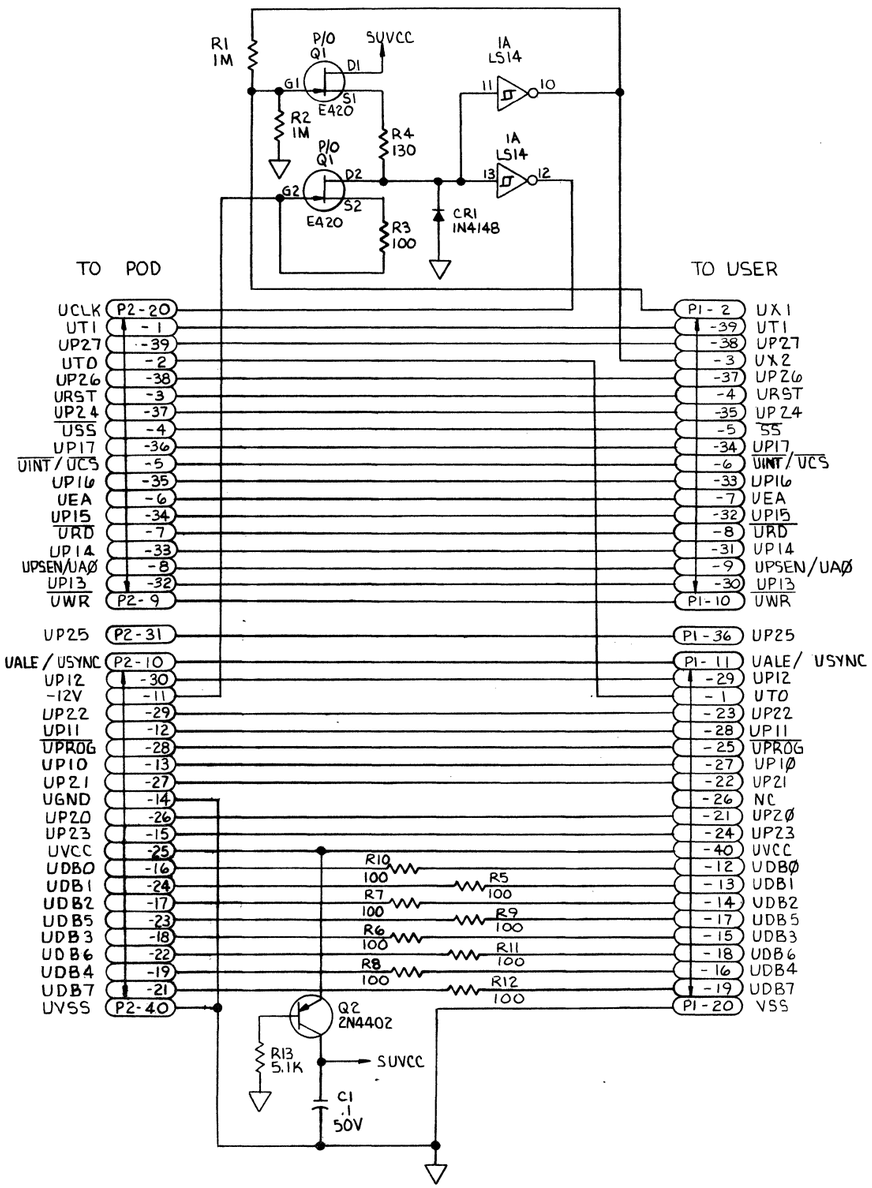
SIZE	FSCM NO.	DWG. NO.	REV.
D		12000154	A

SCALE NONE SHEET 1 OF 1

DWG. NO.	SH	REV.
12000127	1	B

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	01	PROTO-TYPE		
	02	PROTO-TYPE		
	03	PROTO-TYPE		
	50	PILOT RELEASE ECO # 16666	10/15/79	CDL
	52	REVISED PER ECO 1940	3-4-80	CDL
	A	PRODUCTION RELEASE 1963	3-20-80	CDL
	B	PER ECO 2329 MR 12-15-80	11-26-80	



Q1 ORIENTATION
BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTOR VALUES ARE IN OHMS, 1/8W, ± 5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. SOME PINS ARE IDENTIFIED WITH TWO MNUEMONICS. MNEUEMONICS TO LEFT OF SLASH REFER TO 8048 APPLICATION. MNUEMONIC TO RIGHT OF SLASH REFERS TO 8041A APPLICATION. ALL OTHER MNUEMONICS REFER TO BOTH APPLICATIONS.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

13000127	8048 USA
NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± / .XXX ± / ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. SENA	7-17-79
CHECKED R.P. Goldstein	8/24/79
ISSUED	10/19/79

Millennium Systems Inc.

SCHEMATIC,
P8048/8041A

SIZE	FSCM NO.	DWG. NO.	REV.
D		12000127	B

SCALE NONE SHEET 1 OF 1

DWG. NO.	SH	REV.
12000126	1	E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	Ø1	PROTO TYPE		
	Ø2	PROTO-TYPE		
	Ø3	PROTO-TYPE		
	50	PILOT RELEASE ECO # 1666	10/15/79	C.L.
	52	REVISED PER ECO 1940	3-4-80	C.L.
	A	PRODUCTION RELEASE 1963	3-20-80	C.L.
	B	PER ECO 2083	6-6-80	C.L.
	C	PER ECO 2122	6-25-80	C.L.
	D	PER ECO 2216	8-19-80	C.L.
	E	PER ECO 2662	9-11-81	C.L.

NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTOR VALUES ARE IN OHMS AND 1/4 W, 5%.
2. CAPACITORS VALUES ARE IN MICRO-FARADS.
3. SYMBOL ⊳— IS A 5.1K COMMON PULL-UP RESISTOR.
4. RESISTOR PACK (RP) VALUES ARE 68 OHMS.
5. ALL IC'S ARE 74LS.

		112	1C	1
RP16		08	1A	2
R18		00	2D	3
C1				
LAST USED	NOT USED	TYPE	REF. DES.	QTY
REF. DESIGNATION		SPARE GATES		

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J. SENA	7-24-79
CHECKED RFerdinand	8/24/79
ISSUED E Eklund	10/2/79

Millennium Systems Inc.

μSA 8Ø48 SCHEMATIC
EMULATOR INTER-FACE

SIZE	FSCM NO.	DWG. NO.	REV
D		12000126	E

SCALE NONE SHEET 1 OF 5

13000126	8048 μSA
NEXT ASSY	USED ON
APPLICATION	

DWG. NO.	SH.	REV.
12000126	2	E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
SEE SH. 1				

(5B1) RDS 1 2
(5B1) $\overline{8\emptyset2I}$
(3D3) USR EN
(3C8) $\overline{CU\ OUT\ EN}$
(4D1) $\overline{RD}$
(4D1) $\overline{PSEN}$
CUDAT (PZ-15)
$\overline{C\ FETCH}$ (P3-6)
(5B1) DEC$\emptyset$4
(5B1) DEC$\emptyset$3
(5B1) DEC$\emptyset$2
(5B1) DEC$\emptyset$1
(3B3) CU OUT EN
(5A1) $\overline{XNTL}$
$\overline{CS5}$ (P3-7)
$\overline{CEQ}$ (P3-3)
$\overline{CSD}$ (P3-4)
(3B2) $\overline{RST}$
(4C1) ALE
$\overline{CSA}$ (PZ-11)
(4D1) $\overline{PSEN}$

$\overline{CPU\ IN}$ (5C8)
$\overline{8\emptyset2\ IN}$ (5D1)
$\overline{8\emptyset2I}$ (1D8)
$\overline{U\ BUS\ OUT}$ (1B8)
CUDAT (5A6)
$\overline{8\emptyset2\ OUT}$ (5C1)
$\overline{U\ BUS\ IN}$ (1D8)
$\overline{POLTCHEN}$ (1A8)
$\overline{CPU\ OUT}$ (5C8)
$\overline{STR\ POLTCH}$ (4B8)
AN BUS (1B8)
OR BUS (1B8)
$\overline{INPZ}$ (4B8)
$\overline{OUT\ PZ}$ (4B8)
PZ LTCH EN (4C8)
FETCH·PSEN (5D8)
$\overline{FETCH\cdot PSEN}$ (5B8)
$\overline{PZ\ LTCH\ STR}$ (4C8)
DR PZ LTCH (4B8)
ENTO (3C8)
$\overline{ENTO}$ (3B8)

$\overline{PZ\ IN}$
$\overline{PROG\ OUT}$
$\overline{PROG\ IN}$
$\overline{OUT\ LB}$
$\overline{AN\ B}$
$\overline{OR\ B}$
$\overline{INS}$
MOVX
$\overline{OTPZ}$
$\overline{ENTO}$

Millennium Systems Inc.		SIZE D	FSCM NO.	DWG. NO. 12000126	REV E
DRAWN J. SENA					
ISSUED	SCALE NONE	SHEET 2 OF 5			

DWG. NO.	SH.	REV.
12000126	3	E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SH. 1		

(5A1) 8ØZ1
(2D1) CU DAT
UCLK P1-40
R13
(5A1) SLO EN
CEPGRM P2-35
CEXMEM P2-33
CUIN EN P2-14
USS P1-8
CSS P2-28
UINT P1-10
CCLK P2-31
CMODE0 P2-29
(2D8) CU OUT EN
CUOUTEN P2-7
CRST P3-22
(2A2) ENTO
UTO P1-4
(2A2) ENTO
(5A1) 8049
UEA P1-12
C2K P2-25
C1K P2-26
(5A1) 8048
UVCC P1-31
URST P1-6
(5A1) 8ØZ1
UTI P1-2

+5V R4 4.7K
R10 4.7K +5V
+5V R3 620Ω
R15 +5V 620Ω
R2 68Ω
LS367
R9 100K
R5 10K
R12 510Ω
+5V
R1 1K
W1
R6 1K
R8 10K
R7 10K
N.C.

8039
4A
SS
INT
XI
X2
RST
TO
EA
T1
+5V

ENB (4D8)
8ILS97
RPI3 100Ω
P2-19 PCLK
LS98
R17 68Ω
P3-21 CURST
R18 68Ω
P3-20 WLT IN H
USREN (2D8)
EPGRM (4C8)(4D8)
P2-24 REFN EN
RPI3 100Ω

P20 (4C8)
P21 (4C8)
P22 (4C8)
P23 (4C8)
RPI
RP5
RP2
P1-7 UP24
P1-19 UP25
P1-5 UP26
P1-3 UP27

D0 (5D8)
D1 (5D8)
D2 (5D8)
D3 (5D8)
D4 (5C8)
D5 (5C8)
D6 (5C8)
D7 (5C8)

RST (1B8)(2B8)(4B8)
CU OUTEN (2C8)
PSEN EN (4D8)

P2-5 CP FAIL

(1) JUMPER W1 IS FOR MASK OPTION
1. IN FOR MASK PULL-UP RESISTOR OPTION.
2. OUT FOR MASK ZERO CROSS OPTION.

Millennium Systems Inc.	SIZE	FSCM NO.	DWG. NO.	REV.
DRAWN J. SENA	D		12000126	E
ISSUED	SCALE NONE		SHEET 3 OF 5	

DWG. NO.	SH	REV.
12000126	4	E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SH. 1		

(3A3) PSEN EN
(3C3) EPGRM
(3D3) ENB

8Ø39 — PSEN, RU, PROG, WR, ALE — 4A

81LS97 4C, 81LS98 6D, 81LS97 5H, 81LS97 4C, 81LS97 4C, 81LS97 5H

P1-16 UPSEN
P1-20 UALE
P1-14 URD
P1-18 UWR
P3-9 CALE
P3-13 CPSEN
P3-11 CWR
PSEN (2D8)(2A8)
RD (2D8)
ALE (2A8)
P1-25 UPROG
P3-17 CRD

(2B2) P2 LTCH EN
(2B2) P2 LTCH STB

(1A3) A11
(3C3) P23
(1A3) A1Ø
(3C3) P22
(1A3) A9
(3C3) P21
(1A3) A8
(3C3) P2Ø
(3D3) EPGRM

158 5C, 273 5D, 81LS98 4D, 81LS98 6D, 81LS98 4D, 81LS97 4C

RP9 10K → +5V

P1-3Ø UP23
P1-23 UP22
P1-27 UP21
P1-29 UP2Ø
P2-1 CP2Ø
P2-2 CP21
P2-4 CP22
P2-3 CP23

(3B3) RST
(2B2) OUT P2

(2B2) INP2
(2B2) DR P2 LTCH

4A — P1Ø, P11, P12, P13, P14, P15, P16, P17 — GND 2Ø

27 UP1Ø
28 UP11
29 UP12
3Ø UP13
31 UP14
32 UP15
33 UP16
34 UP17

P1-26 UP1Ø
P1-24 UP11
P1-21 UP12
P1-17 UP13
P1-15 UP14
P1-13 UP15
P1-11 UP16
P1-9 UP17

Millennium Systems Inc.	SIZE	FSCM NO.	DWG. NO.	REV
DRAWN J. SENA	D		12000126	E
ISSUED	SCALE NONE			SHEET 4 OF 5

DWG. NO.	SH	REV.
12000126	5	E

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
SEE SH 1				

(2D1) ~~8002~~ IN

(2D1) ~~8002~~ OUT

(2B2) FETCH•PSEN

(3C3) DØ - D7

(2D2) CPU IN

(2C1) CPU OUT

(2B1) FTCH PSEN

RDS2

RDS1

8LS97 3B: DØ D1 D2 D3 → PDØ PD1 PD2 PD3

8LS97 3B: D4 D5 D6 D7 → PD4 PD5 PD6 PD7

8LS97 2B: DØ D1 D2 D3 → PDØ PD1 PD2 PD3

8LS97 2B: D4 D5 D6 D7 → PD4 PD5 PD6 PD7

6349 1B: DØ D1 D2 D3 D4 D5 D6 D7 → PDØ PD1 PD2 PD3 PD4 PD5 PD6 PD7

8LS97 2H: PD7 PD6 PD5 PD4 → RP16-8, RP16-5 → P2-43 CD7, P2-45 CD5

8LS97 1H: PD3 PD2 PD1 PDØ → RP16-3 → P2-47 CD3

8LS97 1H: PD7 PD6 PD5 PD4 → RP15-7, RP15-5 → P2-44 CD6, P2-46 CD4

8LS97 2H: PD3 PD2 PD1 PDØ → RP15-4, RP16-1, RP15-1 → P2-48 CD2, P2-49 CD1, P2-50 CDØ

PD7 (1C8)
PD6 (1C8)
PD5 (1C8)
PD4 (1C8)
PD3 (1B8)
PD2 (1B8)
PD1 (1B8)
PDØ (1B8)

+5V → RP10 10K

2E: 8Ø48 8Ø21 8Ø22 8Ø41 8Ø49 SLOEN XNTL

8LS98 1E

8S115 1F: PD7 PD6 PD5 PD4 PD3 PD2 PD1 PDØ → DECO 4 (2C8), DECO 3 (2C8), DECO 2 (2C8), DECO 1 (2C8)

RP13

8LS97 5H → RP14-7 → P3-15 ILOP

XNTL (2C8)
SLO EN (3D8)
8049 (3B3)
8Ø21 (3D8)(3A8)
8048 (3B8)
RDS1 2 (2D8)

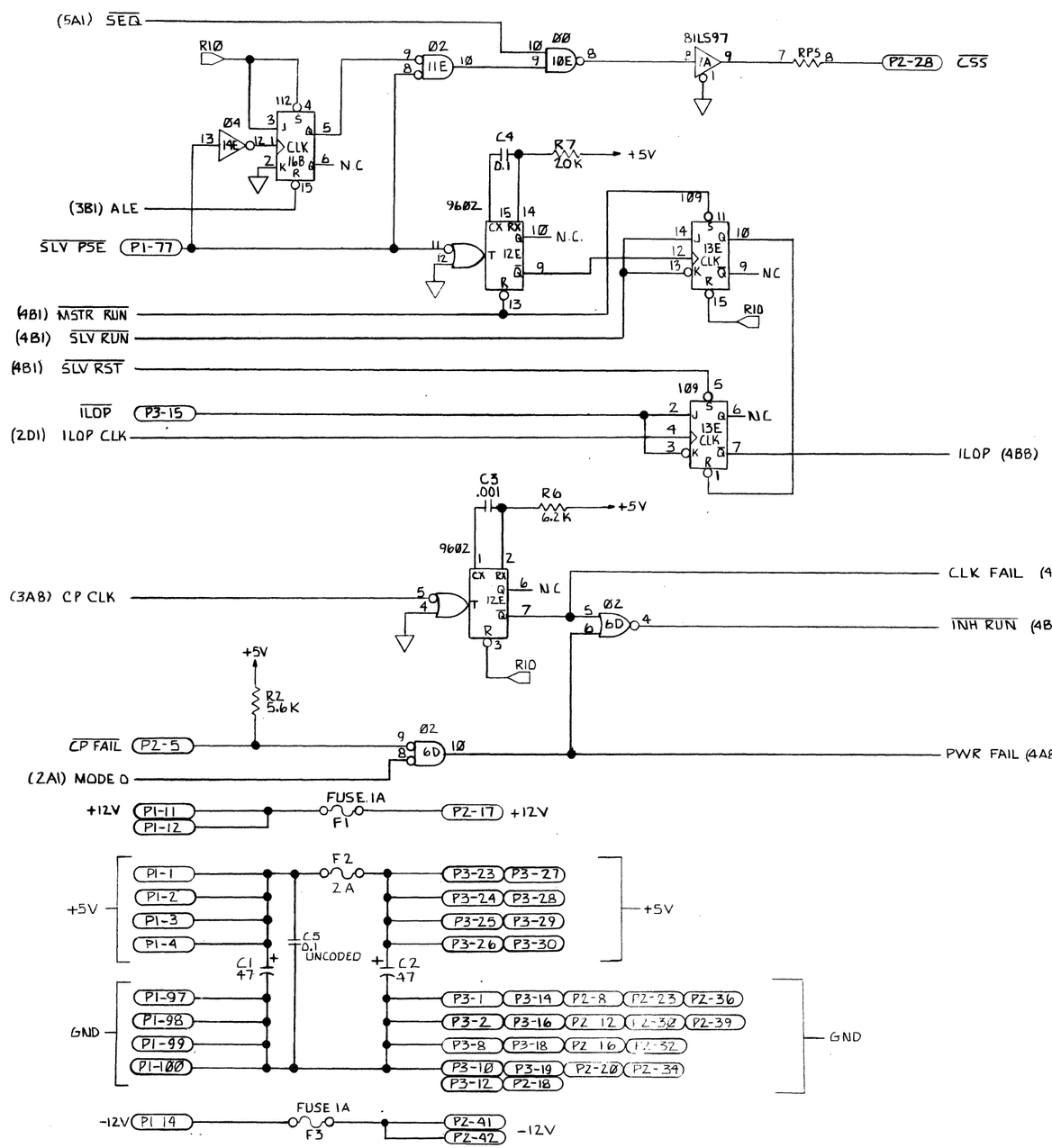
3F

Millennium Systems Inc.		SIZE D	FSCM NO.	DWG. NO. 12000126	REV. E
DRAWN J. SENA					
ISSUED		SCALE NONE		SHEET 5 OF 5	

DWG. NO.	SH	REV.
12000125	1	H

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	E	PER ECO 2304 EB	9/29/80	C. LITTLE
	R	REDRAWN WITHOUT CHG. PER ECO 2317	10/7/80	mw
	F	PER ECO 2337	4-3-81	ACB
	G	PER ECO # 2741	9-16-81	ACB
	H	PER ECO #2805 ADDED R14	1-18-82	



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS AND ¼W, 5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. SYMBOL ▷— IS A 5.6K COMMON PULL-UP RESISTOR.
4. RESISTOR PACK (RP) VALUES ARE 100 OHMS
5. ALL ICS ARE 74LS.

		LS112	16B	1
		81LS98	10A	3
		81LS97	7A	1
		81LS97	6A	3
		LS373	9C	4
		LS273	10C	4
		LS273	3A	1
		LS273	15F	2
		LS86	17A	2
		LS10	16E	1
		7407	9E	2
		LS02	18F	2
		LS02	18D	1
RP7		LS02	7B	1
R14		LS00	1D	2
C4		LS00	16C	1

NEXT ASSY	USED ON	LAST USED	NOT USED	TYPE	REF DES	QTY
12000125	8048 LISA					
FIRST APPLICATION		REF DESIGNATIONS		SPARE GATES		

APPROVALS	DATE
DRAWN JUY THOMPSON	10-7-80
CHECKED	10.9.80
ENGR T. LENNOX	10/12/79

Millennium Systems Inc.

SCHEMATIC
LISA 8048 EMULATOR
PROCESSOR

SIZE	DWG. NO.	REV.
D	12000125	H

SHEET 1 OF 5

DWG. NO.	SH	REV.
12000125	2	H

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SH. 1		

(4B1) INHILOP
(5D1) 1DØ-1D7
(3B1) OP
(5B4) DEC STK PC
(3C1) INT IN PROG
(4D1) RDSO
(5A3) SEQ
(5A1) SEQ JMPACK
(4B1) RST
(3D1) EQ
(3C1) INSTR LTCH
(3B1) OP
(4B1) APP
(4B1) RSTI
(3A1) CSS
(5D1) RST ADD A
(4C1) ROM DIS
(3D1) CYZ
(4C1) MODE O

RIO
RIØ
R14
R12
R3
RST ADD H

14C
11D TMR
11D CNTR
9D MBI
9D C/T INT EN
10D EXT INT EN
14C
6C
6C
8D
81LS97
7C
139
259
273
12D
13D
42
14D
FETCH DECODE 6349
7D

ILOP CLK (1C7)
EX (4D8)
P2-35 CEPGRM
P2-33 CEXMEN
RP5
AUX IO (4D8,3B8)
ROM DIS (4A8)(4B8)
E INHOP (3B8)
RST ADD H (5B8)
RST ADD A (5B8)
A12 (5C8)
MODE O (1B7)
RET (3B8)
DD1 (3C8)
DDO (3C8)

NC
N.C.
MOVXRO
MOVXRI
NPMOVXRI
NP

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Millennium Systems Inc.	SIZE	FSCM NO.	DWG. NO.	REV.
DRAWN J. SENA	D		12000125	H
ISSUED	SCALE NONE		SHEET 2 OF 5	

(4B1) RST
(4A1) INT VECT
(4B1) RSTŹ
SYS CLK P1-96
(5D1) IDO
(2A1) DDØ
(2A1) DD1
C ALE P3-9
P CLK P2-19
C WR P3-11
C RD P3-17
C PSEN P3-13
(4C1) UDAT
(2B1) E INHOP
(5A1) S INHOP
(2B1) AUX IO
(4C1) UDAT
(4D1) RDS2
(2A1) RET
(4B1) SLV RUN
(5A1) JACK
(4C1) ACTIVE
REFNEN P2-24
(1B7) CP CLK
(4B1) RST2
(4B1) MRST

81LS97 9A RP6 4
R4 109 11B 10 NC
109 10B FTCH
Ø2 15B 4
16B 10 12 NC
109 16A R10 N/C
86 17A Ø0 17B
109 14B 10 NC
109 R9 Ø2 12C
109 R10 13C Ø2 12C RST·ALE
EQ (2C8) (5A8)
109 FTCH LST NC
RST·ALE
109 13C 81LS98 10A P3-34 CIIP
INT IN PROG (2D8)
139 9B FTCH RD NC WRT NOBYT
109 10B 10
109 11B VMA NC
Ø0 17B
PSEN (5B8) (4B8)
INSTR LTCH (2C8)
81LS97 9A RP6 P3-3 CEQ
EQ (5A8)
81LS97 9A Ø4 15A
112 13B R9
Ø2 15B
Ø0 8A
Ø0 1B
Ø0 8B
Ø4 14E
Ø2 12C 10
Ø2 7B 10
20 12B
368 8E
+5V R11 5.6K R13 5.6K
Ø4 15A
Ø4 68
CS7
Ø0 8B
Ø2 15B
PI-55 R/W
PI-75 SLV OP REQ
PI-54 DP REQ
PI-60 JACK
PI-53 WRP
PI-52 IO/MEM
R/W (4C8)
OP REQ (4C8)
WRP (4C8)
IO/MEM (4C8)
OP (2D8) (5B8)
PSEN (4B8)
(PSEN+RD) UDAT (5C8)
OP (2B8)
81LS97 9A RP6 P3-6 C FETCH
Ø0 17D
(PSEN+RD) UDAT (5D8) (4A8)
WR (5B8)
ALE (5C8) (1C7)
7407 9E PI-78 REFN
PI-82 FETCH
PI-93 SLV CLK
11C 10
Ø4 15A
368 5E
PHALT (4B8)
CS5 (2B8)
CS5
81LS98 10A CSD CSB CSA CS5
RP7 5
RP7 3
RP7 1
RP7 7
P3-4 CSD
P3-5 CSB
P2-11 CSA
P3-7 CS5
164 12A 164 11A
CSA CSB CSD

Millennium Systems Inc.
DRAWN J. SENA
ISSUED
SIZE D | FSCM NO. | DWG. NO. 12000125 | REV. H
SCALE NONE | SHEET 3 OF 5

DWG. NO.	SH	REV
12000125	4	H

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED

SEE SH. 1

(2B1) AUX IO
(3D3) RD + WR + PSEN
(2C1) EX
(5B1) AØ - AIØ
MAP
MST RUN
(3B1) OP REQ
(3B1) IO / MEM
(3B1) WRP
(3C1) R / W
PRST
USA FRST
(1C3) ILOP
(3B1) PSEN
(5A3) JARM + ALE
(5A3) SEQ
(2B1) ROM DIS
SLV RST
CURST
(1B3) INHRUN
(5B1) AII
(3A1) PHALT
HLT INH
(5D1) IDØ - ID7
(3C1) PSEN
CMEM
(5A3) SEQ
(5C1) D BUS OUT
(5A3) SEQ + JMP SVC
(3B1) (PSEN + RD) UDAT
(1B3) CLK FAIL
(1B3) PWR FAIL
CP23
CP22
CP21
CP2Ø
(2B1) ROM DIS

P1-9Ø
P1-84
P1-59
P1-72
P1-76
P3-21
P3-20
P1-33
P2-4
P2-3
P2-2
P2-1

RDSØ (2D8)
P2-37 RD51
RD52 (3B8)
P2-38 RD52
WAUX (5A8)
AØ - AIØ (5D8)
SMB (5C8)
SCNT (5C8)
SWTY (5C8)
P2-7 C UOUTEN
P2-15 C UDAT
UDAT (3B8)
UDAT (3B8)
ACTIVE (3B8)
MODE Ø (2A8)
P2-29 C MODE Ø
P2-14 C UINEN
DBG (5B8)
ROM DIS (2A8)(5B8)
MSTR RUN (1C7)
APP (2B8)
RETU (5C8)
RETU (5A8)
SLV RST (1C7)
IN HILOP (2D8)
MRST (3A8)
MRST (5A8)
RST 1 (2B8)
P3-22 CRST
RST (2C8)(3D8)(5A8)
RST 2 (3A8)(3D8)
SLV RUN (5C8)
SLV RUN (1C7)(3B8)(5B8)
P1-58 RUN
DAT BUS OUT (5D8)
CE (5D8)
P1-34 RAM INH
DAT BUSIN (5D8)
INT VECT (3D8)
CPZØ - CP22, TP23 (5A8)

R5 5.6K +5V
R8 5.6K +5V
RP1
RP4
RP5
MODE 2
MSTR CMD
APP
MRST
ACTIVE
NC

Millennium Systems Inc.	SIZE D
DRAWN J. SENA	FSCM NO.
ISSUED	DWG. NO. 12000125
SCALE NONE	REV. H
	SHEET 4 OF 5

DWG. NO.	SH	REV.
12000125	5	H

REVISIONS			
ZONE	REV.	DESCRIPTION	DATE	APPROVED

(4AI) DAT BUS OUT
(4AI) DAT BUS IN
(4DI) AØ - A1Ø
(4AI) CE

RST ADD A (2A8)
1DØ-1D7(2D8) (4B8)
(3D8)

(3BI) (PSEN+RD) UDAT

(CD7) P2-43
(CD6) P2-44
(CD5) P2-45
(CD4) P2-46
(CD3) P2-47
(CD2) P2-48
(CD1) P2-49
(CDØ) P2-5Ø

(3BI) (PSEN+RD) UDAT

(4BI) SLV RUN
(3BI) ALE
(3BI) WR
(2AI) A12
(4DI) SWTY
(4DI) SCNT
(4DI) SMB
(4BI) JMP SVC RETU
(4CI) DBG
(4CI) ROM DIS
(3CI) PSEN

(3BI) SLV RUN
(2AI) RST ADD A
(2BI) RST ADD H

(3BI) OP

JMP CMD P1-57

(4BI) MRST
(3DI) FTCH·ALE
(4BI) RST
(3DI) EQ
(3CI) EQ
(4DI) WAUX

(4AI) CP2Ø-CP2?, TP23
(3DI) ALE

(4BI) RETU

JMP SEQUENCER

D BUS OUT (4A8)

P1-43 D7
P1-42 D6
P1-41 D5
P1-4Ø D4
P1-39 D3
P1-38 D2
P1-37 D1
P1-36 DØ

P2-26 C1K
P2-25 C2K

P1-24 A7
P1-23 A6
P1-22 A5
P1-21 A4
P1-2Ø A3
P1-19 A2
P1-18 A1
P1-17 AØ

AØ - A1Ø (4D8)
A11 (4B8)

P1-28 A11
P1-27 A1Ø
P1-26 A9
P1-25 A8

SINHOP (3B8)

P1-32 A15
P1-31 A14
P1-3Ø A13
P1-29 A12
JACK (3B8)

DEC STK PC (2D8)
SEQ JMP ACK (2C8)
SEQ (4B8) (1D7)

SEQ (4A8) (2C8)
JARM + ALE (4B8)
SEQ + JMP SVC (4A8)

Millennium Systems Inc.	SIZE	FSCM NO.	DWG. NO.	REV.
DRAWN J. SENA	D		12000125	H
ISSUED	SCALE NONE		SHEET 5 OF 5	

DOCUMENT REVIEW FORM

9508 MICROSYSTEM EMULATOR
USERS MANUAL ADDENDUM
8048/49/21/41A EMULATOR OPTION

Publication No. 87000077
September 1981
Release 1.0

Dear Customer:

Your comments concerning this document will help us to produce better documentation for you.

GENERAL COMMENTS

- ☐ Easy to read?
- ☐ Complete?
- ☐ Well organized?
- ☐ Well illustrated?
- ☐ Accurate?
- ☐ Suitable for your needs?

SPECIFIC COMMENTS AND CORRECTIONS

Reference	Page

Please send your comments to:

Millennium Systems, Inc.
19050 Pruneridge Avenue
Cupertino, Calif. 95014
ATTN: Publications

MILLENNIUM SYSTEMS, INC.

PRODUCT ENHANCEMENT REQUEST

1. DATE

2. CUSTOMER INFORMATION

   NAME OF COMPANY
   NAME OF EMPLOYEE
   ADDRESS
   CITY/STATE/ZIP CODE
   PHONE # _____ EXT. _____

3. PRODUCT NAME (9508, 9520, 9516, 9580, ETC.)

4. DESCRIPTION OF ENHANCEMENT

5. DESCRIPTION OF HOW ENHANCEMENT WOULD BE USED

6. HOW LONG BEFORE YOU MUST HAVE THIS ENHANCEMENT?

   NOW _____
   6 MONTHS _____
   1 YEAR _____
   2 YEARS _____

7. WHAT SHOULD BE THE COST OF THIS ENHANCEMENT?

(ATTACH ADDITIONAL SHEETS AS REQUIRED)

MILLENNIUM SYSTEMS, INC.

SOFTWARE/SYSTEM PROBLEM REPORT

1. DATE

2. CUSTOMER INFORMATION

   NAME OF COMPANY
   NAME OF EMPLOYEE
   ADDRESS — TELEPHONE # _____
   CITY/STATE/ZIP CODE — EXTENSION _____

3. HARDWARE/SOFTWARE CONFIGURATION

   9520

   SERIAL # _____ VOLTAGE _____ HERTZ _____
   MEMORY SIZE: 64K? _____ 112K? _____
   OPERATION SYSTEM _____ VERSION # _____

   9508

   SERIAL # _____ VERSION # _____
   16K? _____
   EMULATOR Z80 _____
   OTHER _____

8080 _____	6800 _____
8085 _____	6801 _____
8048/49 _____	6802 _____
8021 _____	6809 _____
8041 _____	

4. HOW ARE THE HOST, 9508, AND UNIT UNDER TEST CONNECTED? PLEASE INDICATE PORT NUMBERS

5. COMMAND OR PROGRAM WHERE PROBLEM OCCURS

   NAME _____ VERSION # _____

6. AFTER POWER ON/RESET, WHAT COMMAND OR SERIES OF COMMANDS WILL REPRODUCE THE ERROR.

7. DESCRIPTION OF THE ERROR

8. PLEASE ATTACH AS MUCH OF THIS OTHER HELPFUL INFORMATION AS POSSIBLE

   SOURCE FILES _____ OBJECT FILES _____
   COMMAND FILES _____ LISTINGS _____
   CONSOLE HARDCOPY _____

(ATTACH ADDITIONAL SHEETS AS REQUIRED)